CB-3 LOGIC SCHEMATICS

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88.DC/DC VCC1R5VIDEO(VT356)
89.DC/DC VCC1R05VIDEO_PLL(BD3551HFN)
90.DC/DC VCC1R8B(BD9139)
91.BLANK
92.DC/DC VCC1R5B(BD3551HFN)
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94.LOAD SW LAN
95.LOAD SW VIDEO
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97.BLANK
98.LOAD SW WWAN & WLAN
99.PTH FOR SCREW HOLES
100.3rd USB

lenovo

Project Name :	Title : TITLE PAGE
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EC Modify History

Date	EC version	File name
2012/10/02	CB_1_SWG_SDV_EC001-009	JV_CB-1_SWG_SDV1_SCH_EC001-008_121001A.pdf
2012/10/05	CB_1_SWG_SDV_EC010	JV_CB-1_SWG_SDV1_SCH_EC001-009_121004A.pdf
2012/10/09	CB_1_SWG_SDV_EC011	JV_CB-1_SWG_SDV1_SCH_EC009-010_100801.pdf
2012/10/12	CB_1_SWG_SDV_EC012	JV_CB-1_SWG_SDV1_SCH_EC010-011_101101.pdf
2012/10/13	CB_1_SWG_SDV_EC013	JV_CB-1_SWG_SDV1_SCH_EC011-012_101201.pdf
2012/10/16	CB_1_SWG_SDV_EC014	JV_CB-1_SWG_SDV1_SCH_EC013_101501.pdf
2012/10/17	CB_1_SWG_SDV_EC015	JV_CB-1_SWG_SDV1_SCH_EC014_101601.pdf
2012/10/18	CB_1_SWG_SDV_EC016	JV_CB-1_SWG_SDV1_SCH_EC015_101701.pdf
2012/10/19	CB_1_SWG_SDV_EC017	JV_CB-1_SWG_SDV1_SCH_EC016_101801.pdf
2012/10/20	CB_1_SWG_SDV_EC018	JV_CB-1_SWG_SDV1_SCH_EC017_101901.pdf
2012/10/25	CB_1_SWG_SDV_EC018-022	JV_CB-1_SWG_SDV1_SCH_EC018-021_102401.pdf
2012/10/31	CB_1_SWG_SDV_EC023	JV_CB-1_SWG_SDV1_SCH_EC022_103001.pdf
2012/10/32	CB_1_SWG_SDV_EC023-025	JV_CB-1_SWG_SDV1_SCH_EC023-024_103101.pdf
2012/11/15	CB_1_SWG_SDV_EC025-033	JV_CB-1_SWG_SDV1_SCH_EC025-032_111401.pdf
2012/11/23	CB_1_SWG_SDV_EC033-036	JV_CB-1_SWG_SDV1_SCH_EC025-035_112201.pdf
2012/11/27	CB_1_SWG_SDV_EC037	JV_CB-1_SWG_SDV1_SCH_EC036_112601.pdf
2012/12/05	CB_1_SWG_SDV_EC037-039	JV_CB-1_SWG_SDV_SCH_EC037-038_120401.pdf

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Title: EC HISTORY

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Custom	COBAIN2 SWG	0.1

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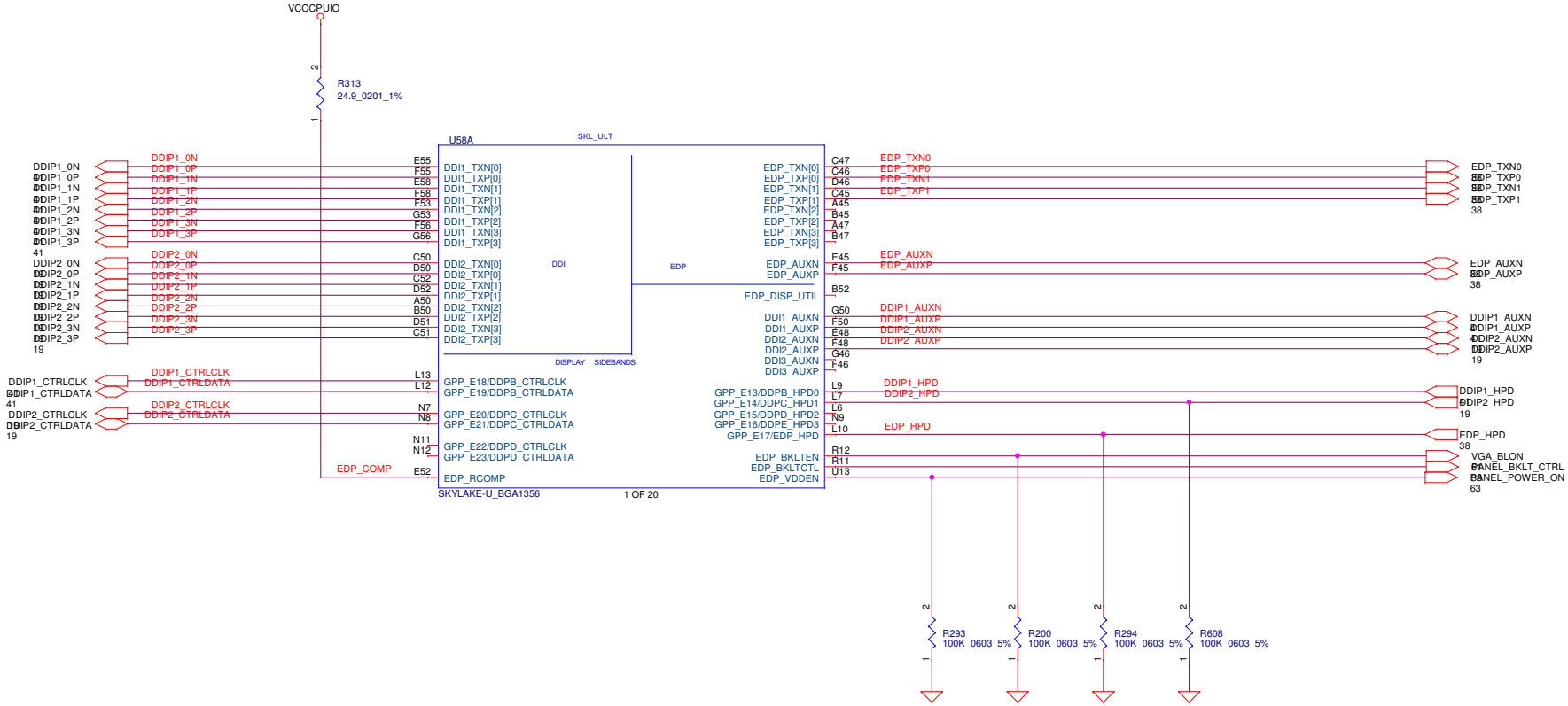

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Title: CPU(1/16) : DDI/EDP

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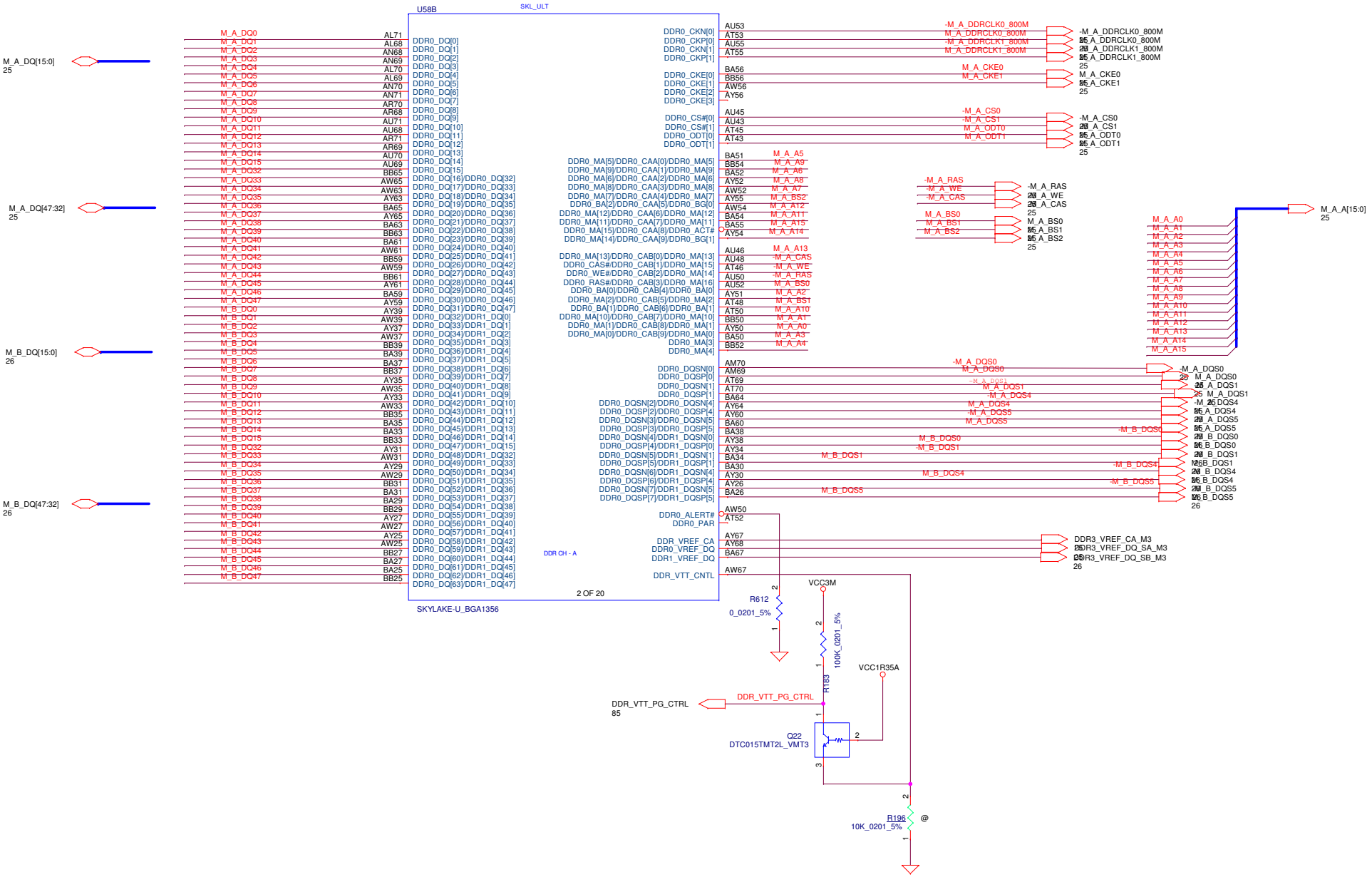

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Title: CPU(2/16) : MISC/JTAG

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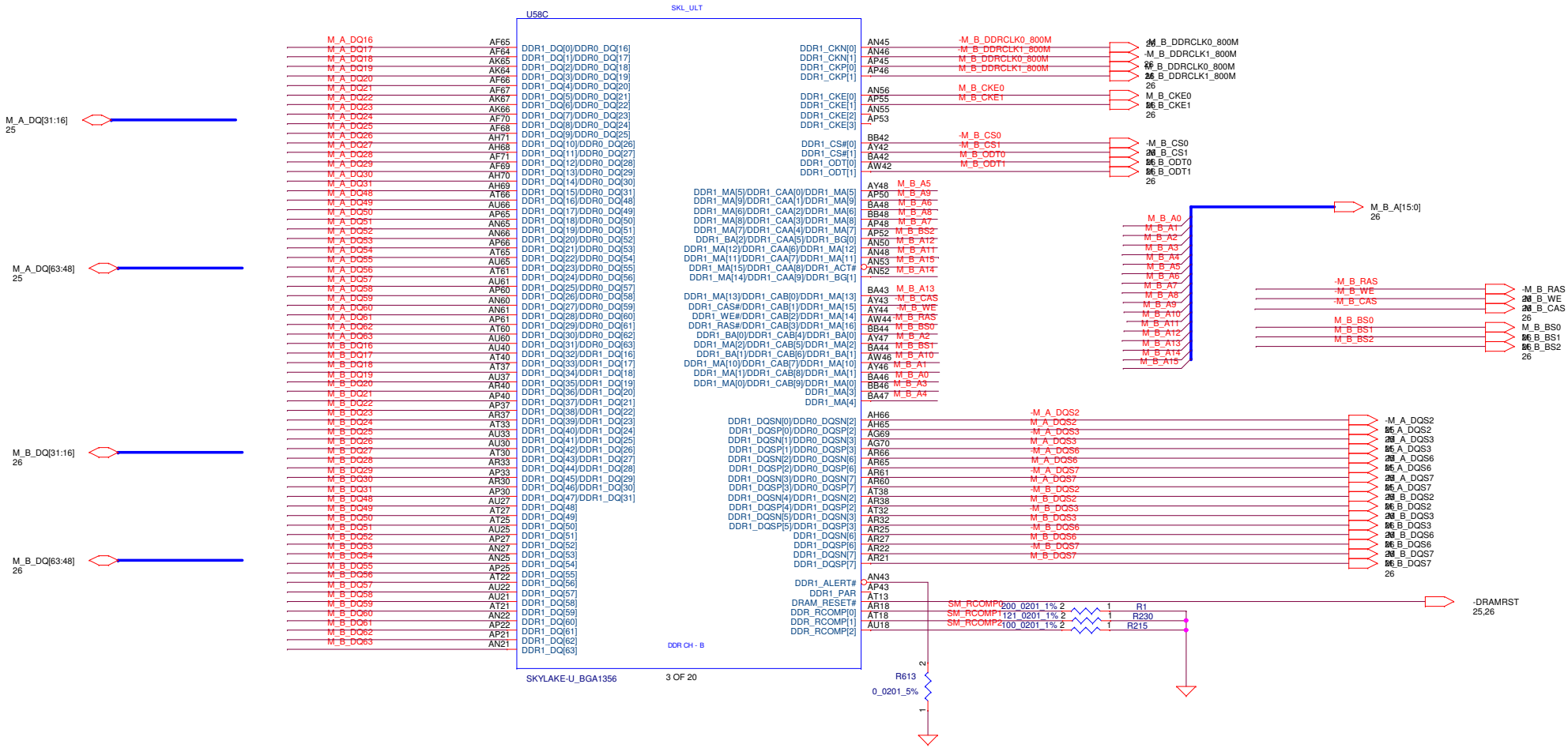

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Title: CPU(3/16) : DDR3L CHANNEL-A

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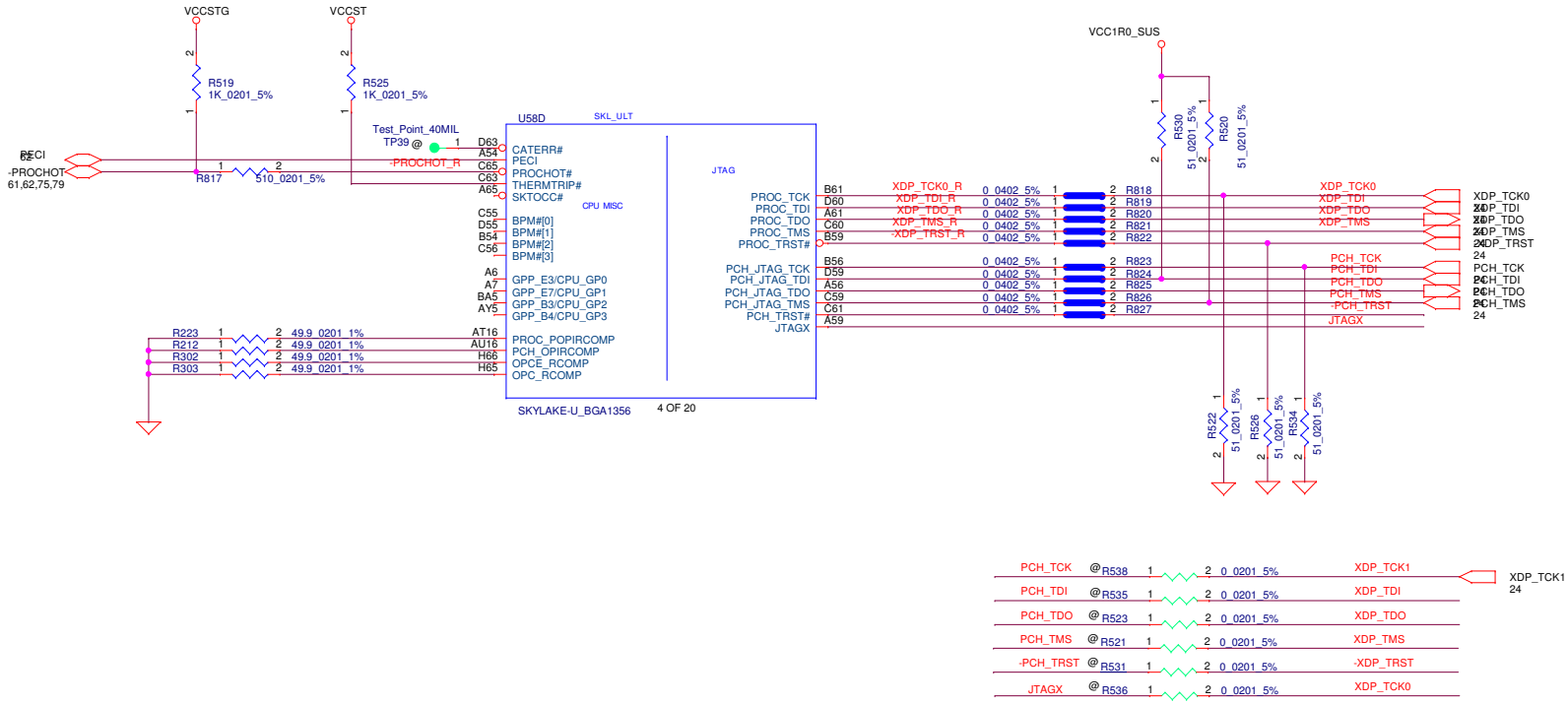

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Title: CPU(4/16) : MISC/JTAG

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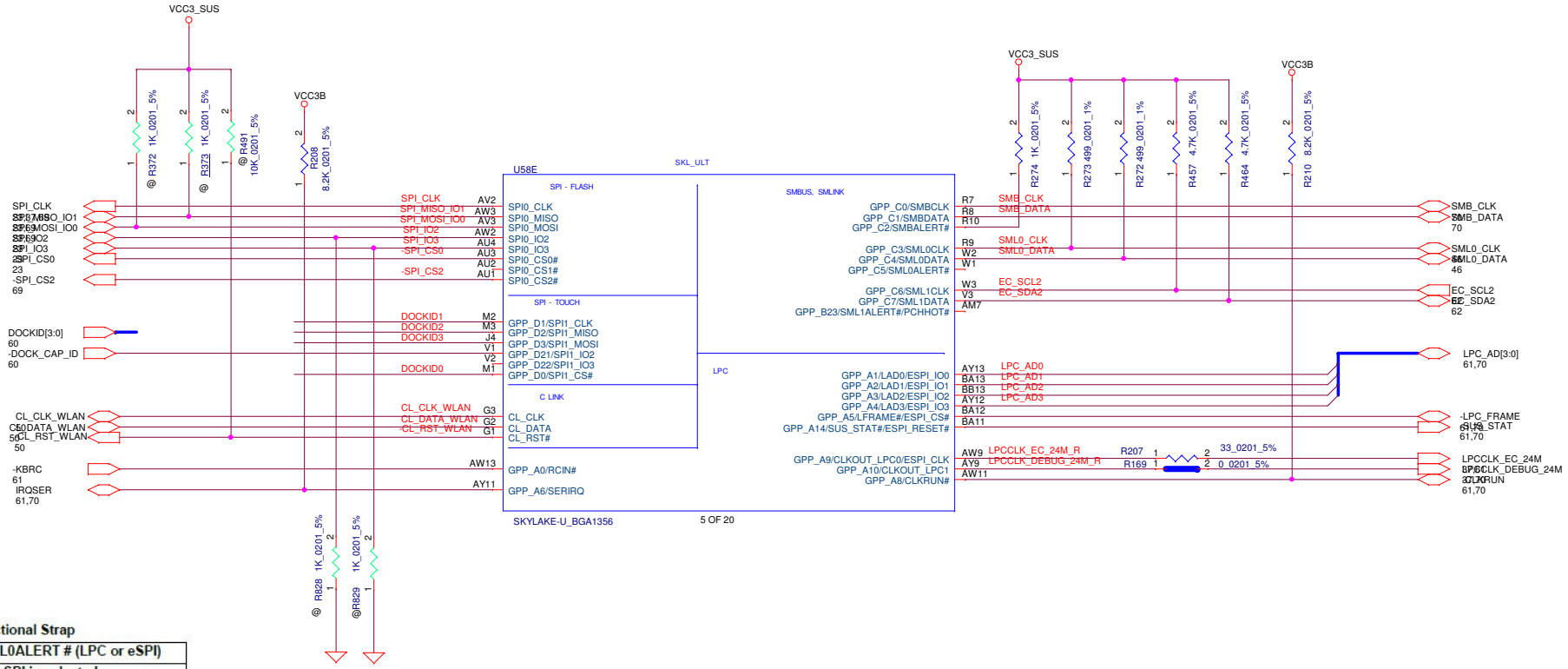

TABLE : Functional Strap

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

<- LOGIC

TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

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Title: CPU(5/16) : LPC/SPI/SMBUS/C

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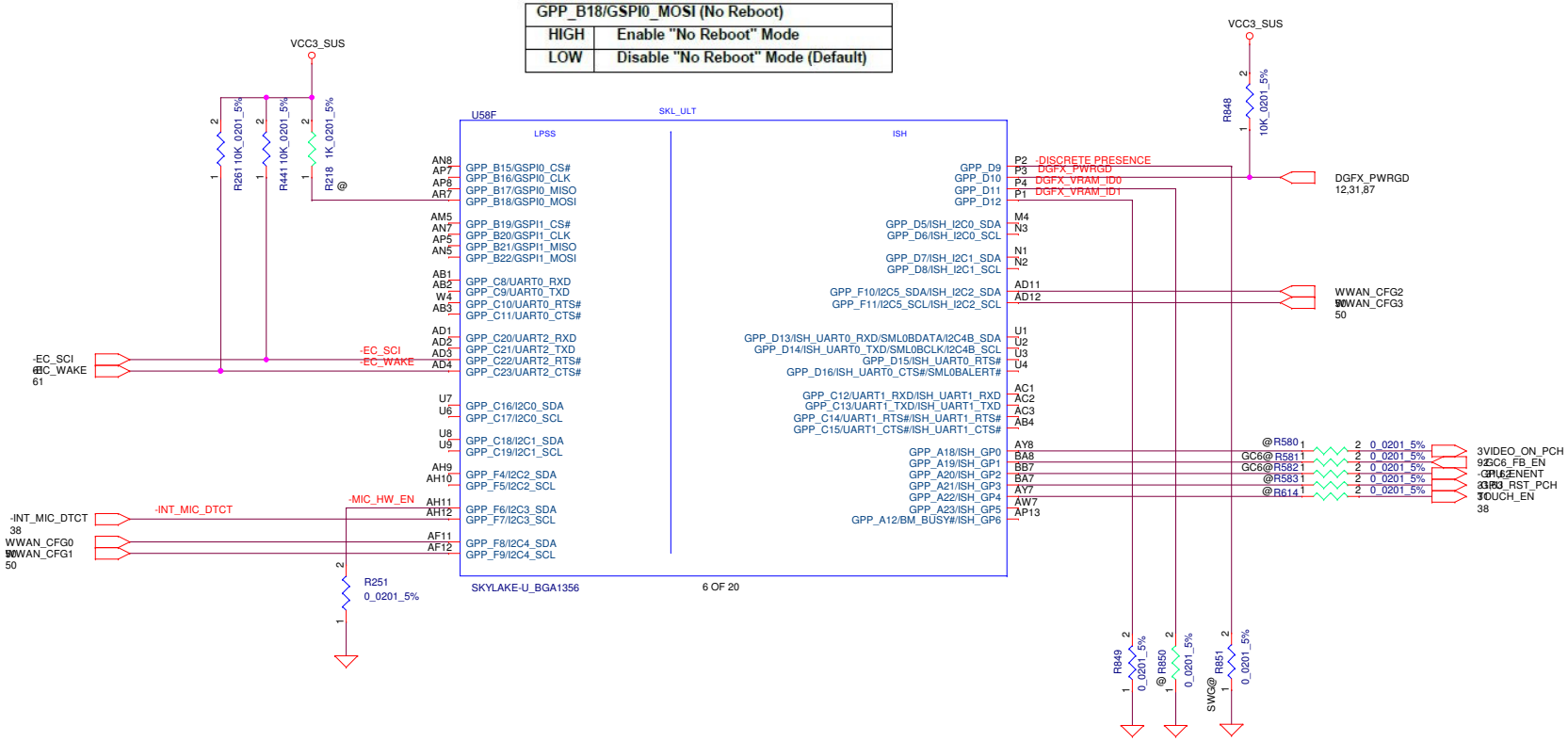
TABLE : Functional Strap

GPP_B22/GSPI1_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)



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Title: CPU(6/16) : LPSS/ISH

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Custom	COBAIN3	0.1

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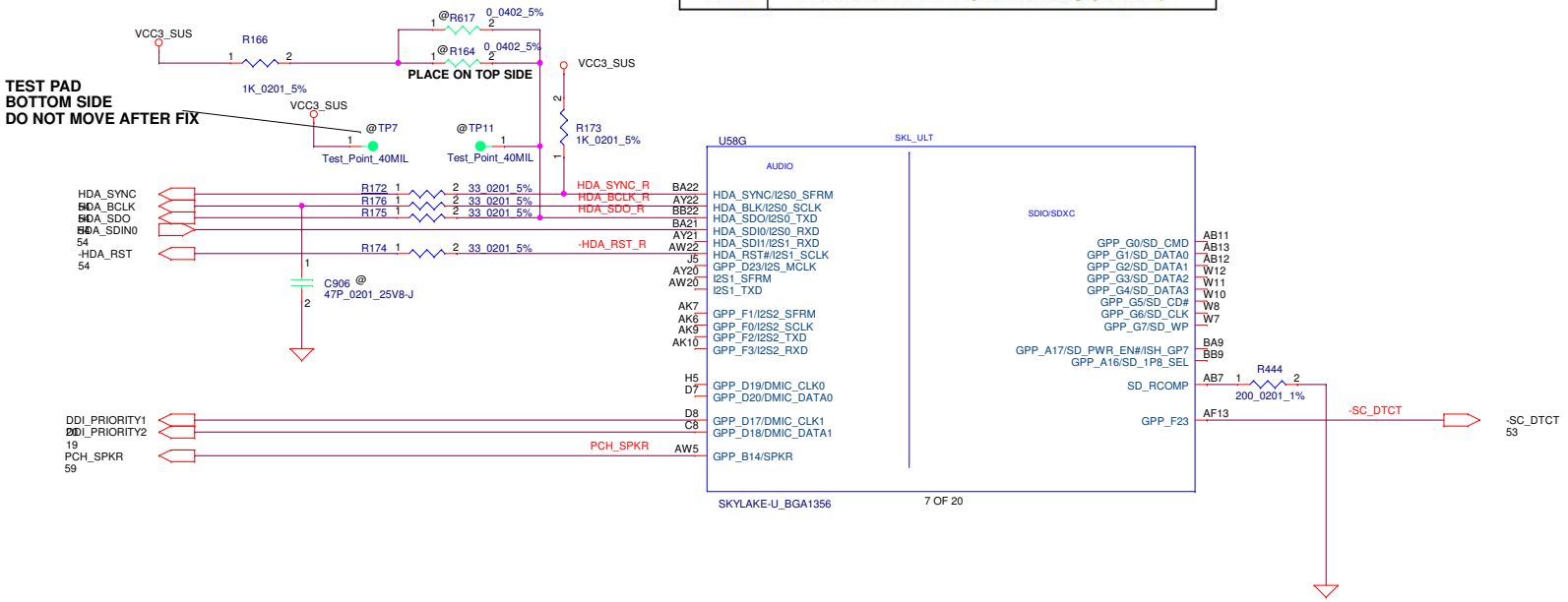
TABLE : Functional Strap

HDA_SDO/I2S0_TXD Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)



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Title: CPU(7/16) : AUDIO/SDXC

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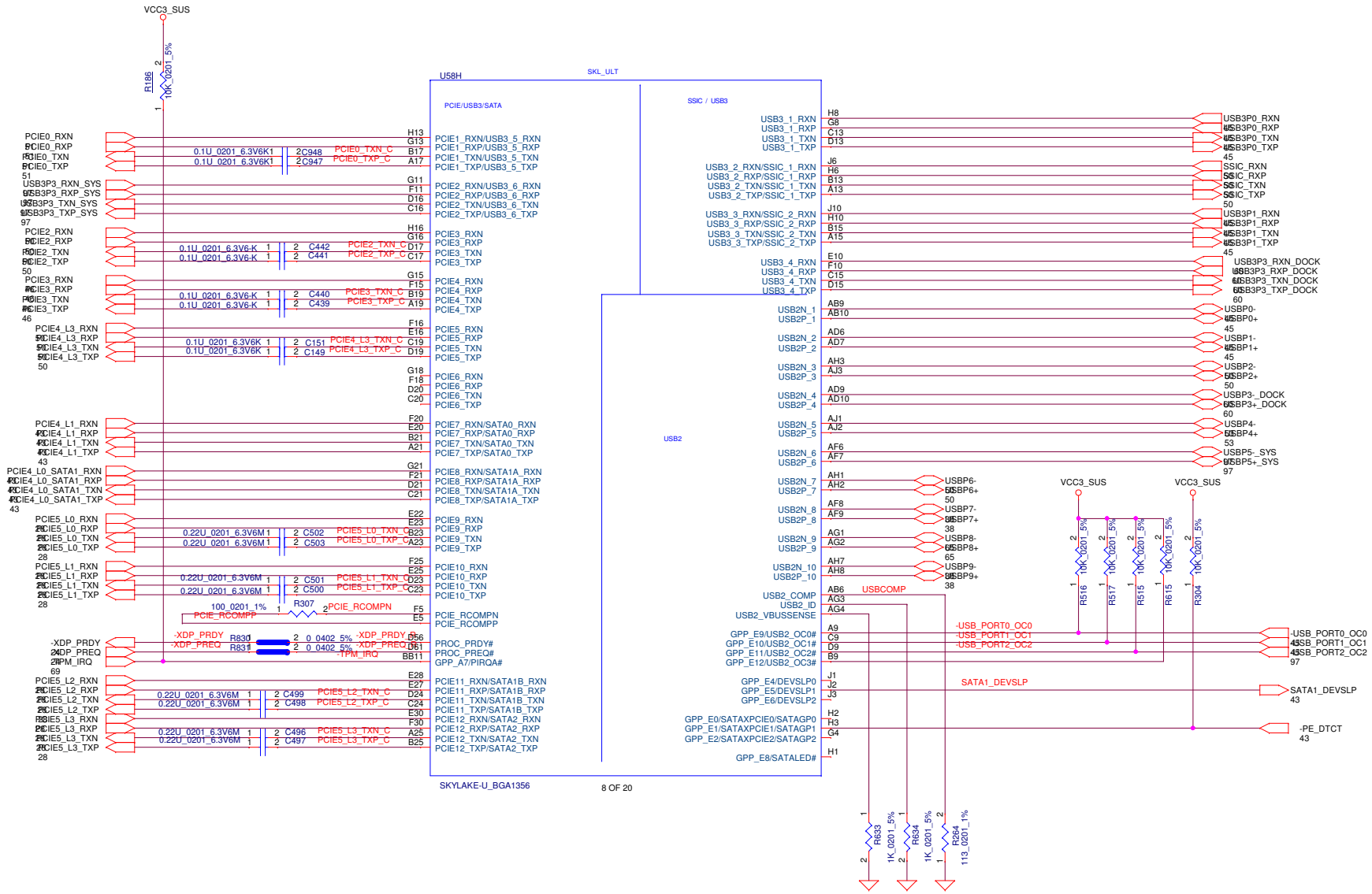

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Title: CPU(8/16) : SYSTEM PM

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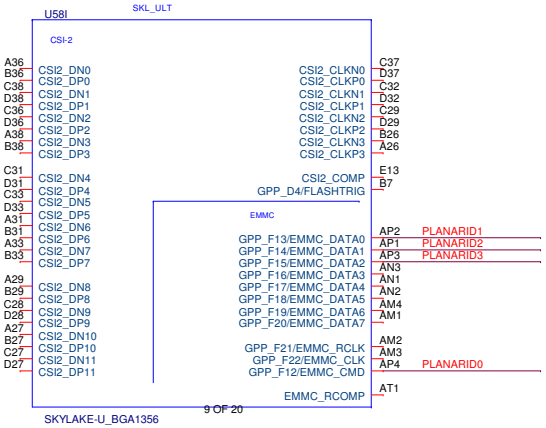

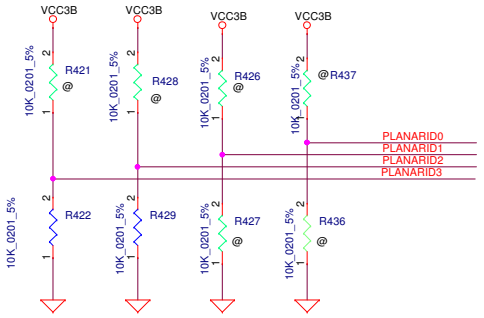

PLANAR ID TABLE		
LEVEL		PLANARID[3..0]
UMA	SWG	
SDV		0000B
FVT		0001B
SIT	FVT	0010B
SVT	SIT	0011B
	SVT	0100B

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Title: CPU(9/16) : CSI-2/EMMC

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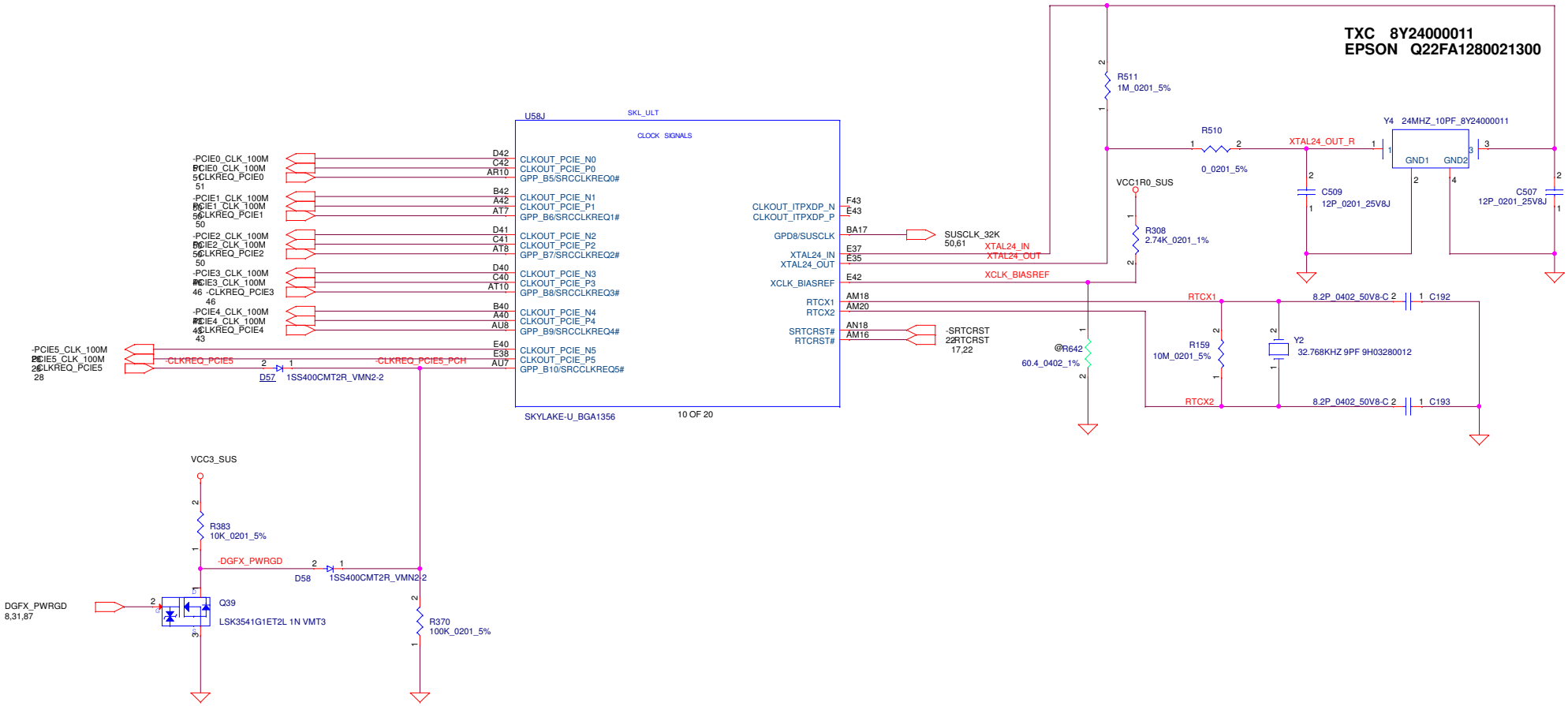

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Title: CPU(10/16) : CLOCK SIGNALS

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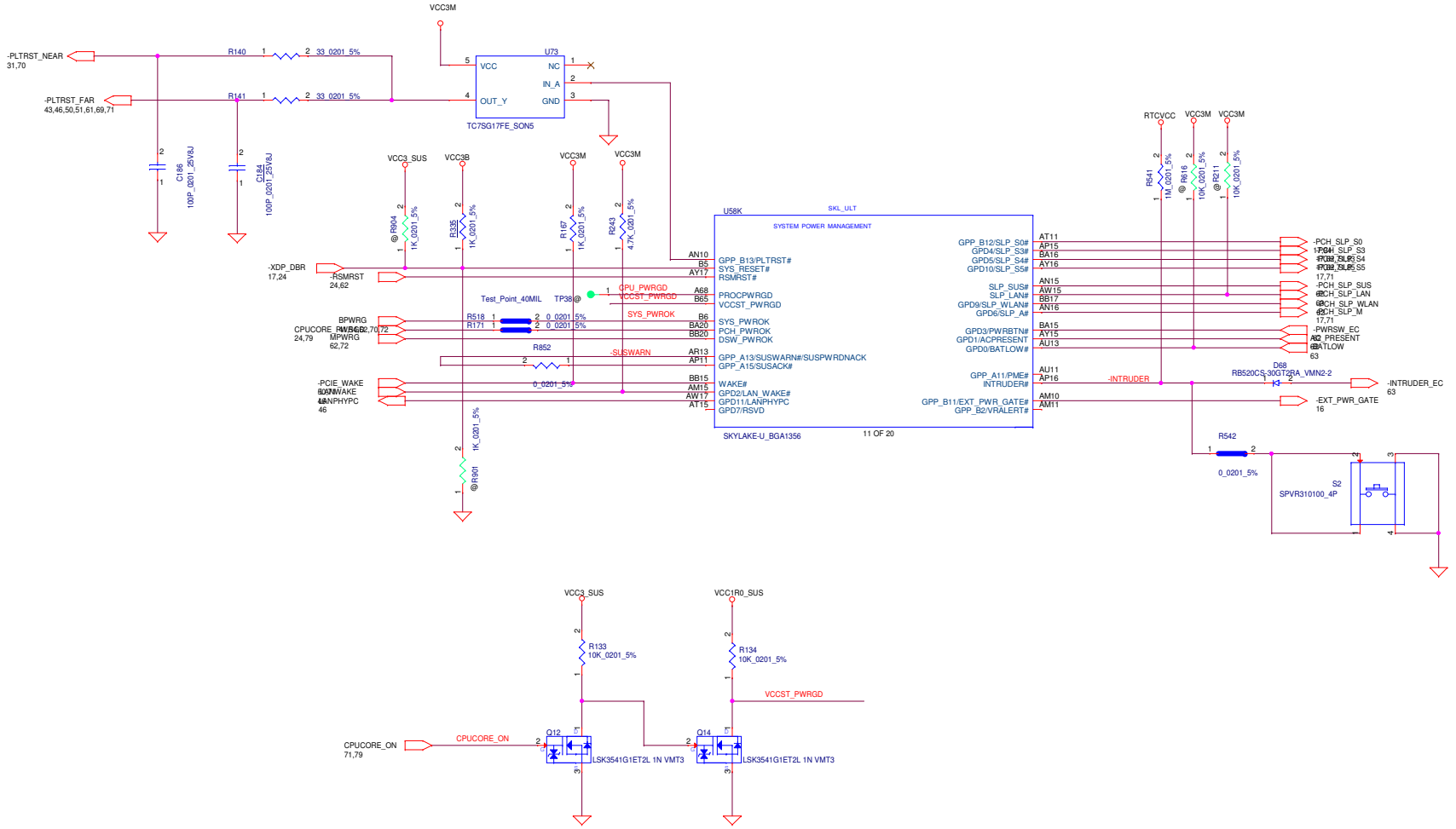

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Title	CPU(11/16) : SYSTEM PM		
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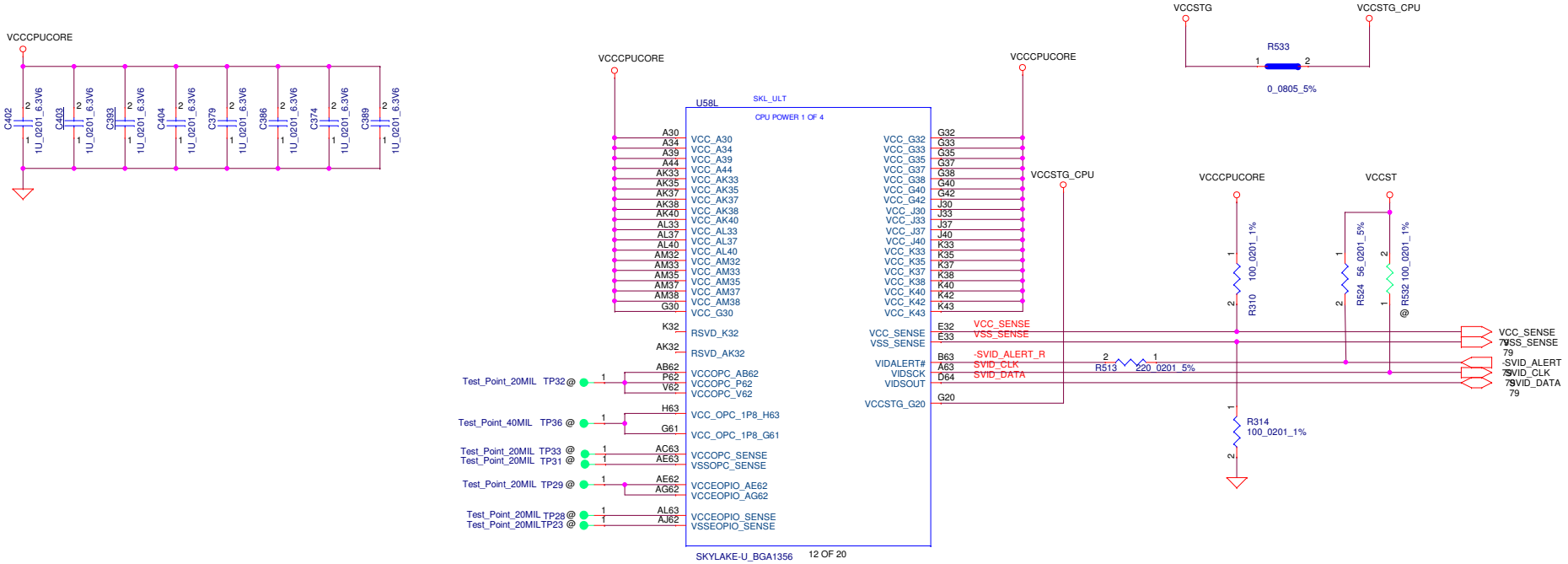

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Title: CPU(12/16) : CPU POWER

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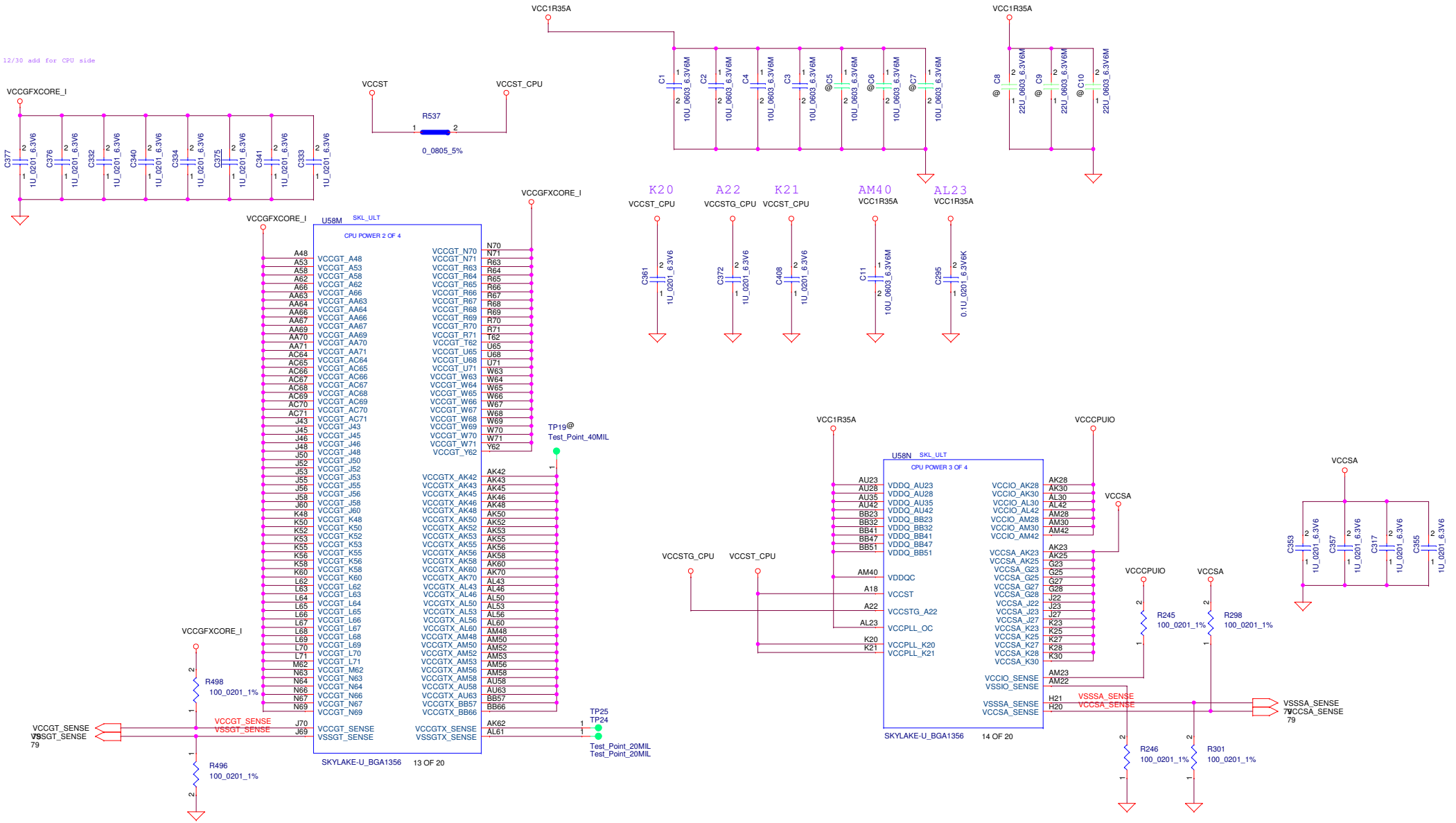

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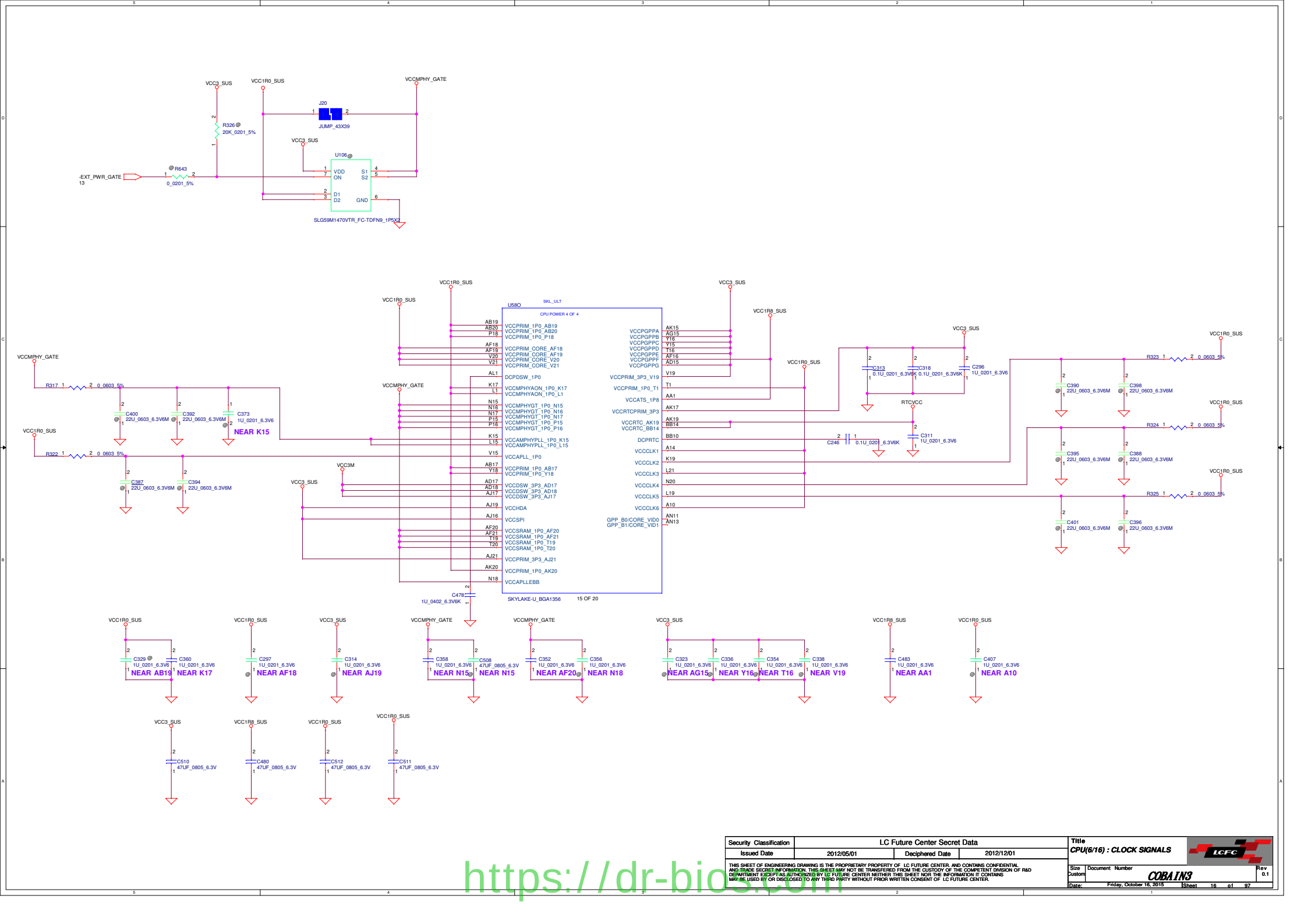

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Title: CPU(6/16) : CLOCK SIGNALS

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Custom	COBAIN3	0.1

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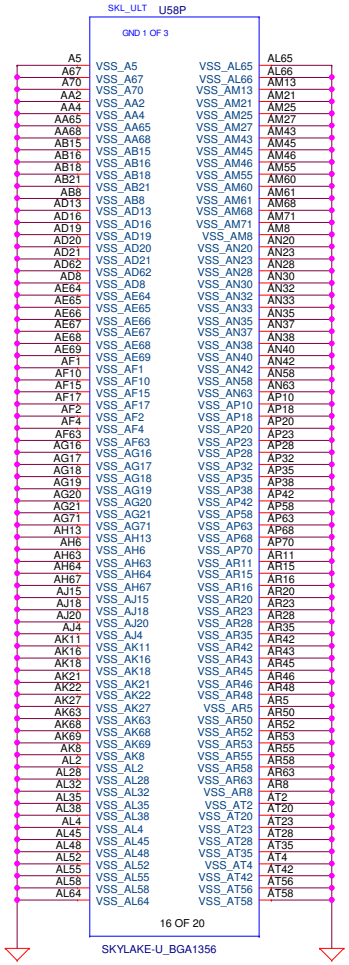
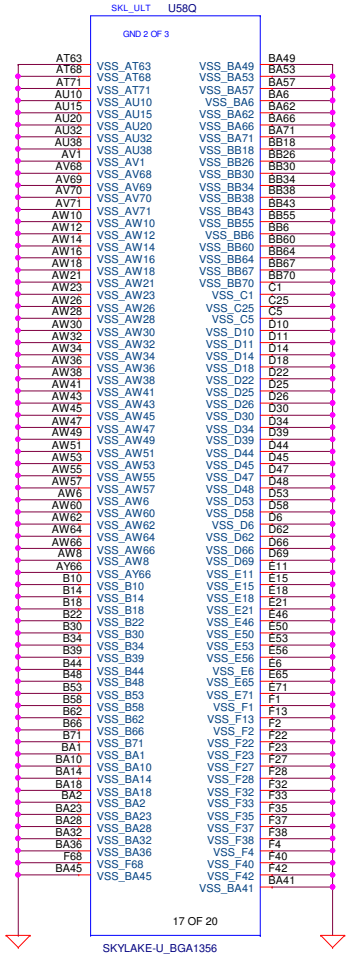
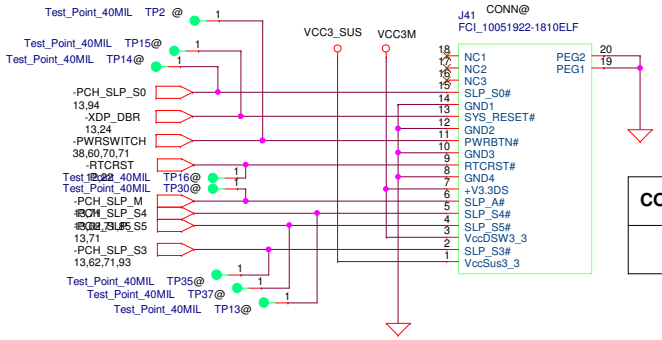
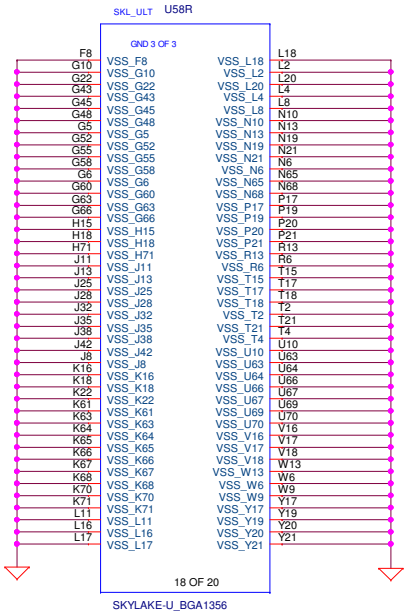




APS/PETS interface



CONNECTOR	Planar Only	BOX
J41	ASM	NO ASM



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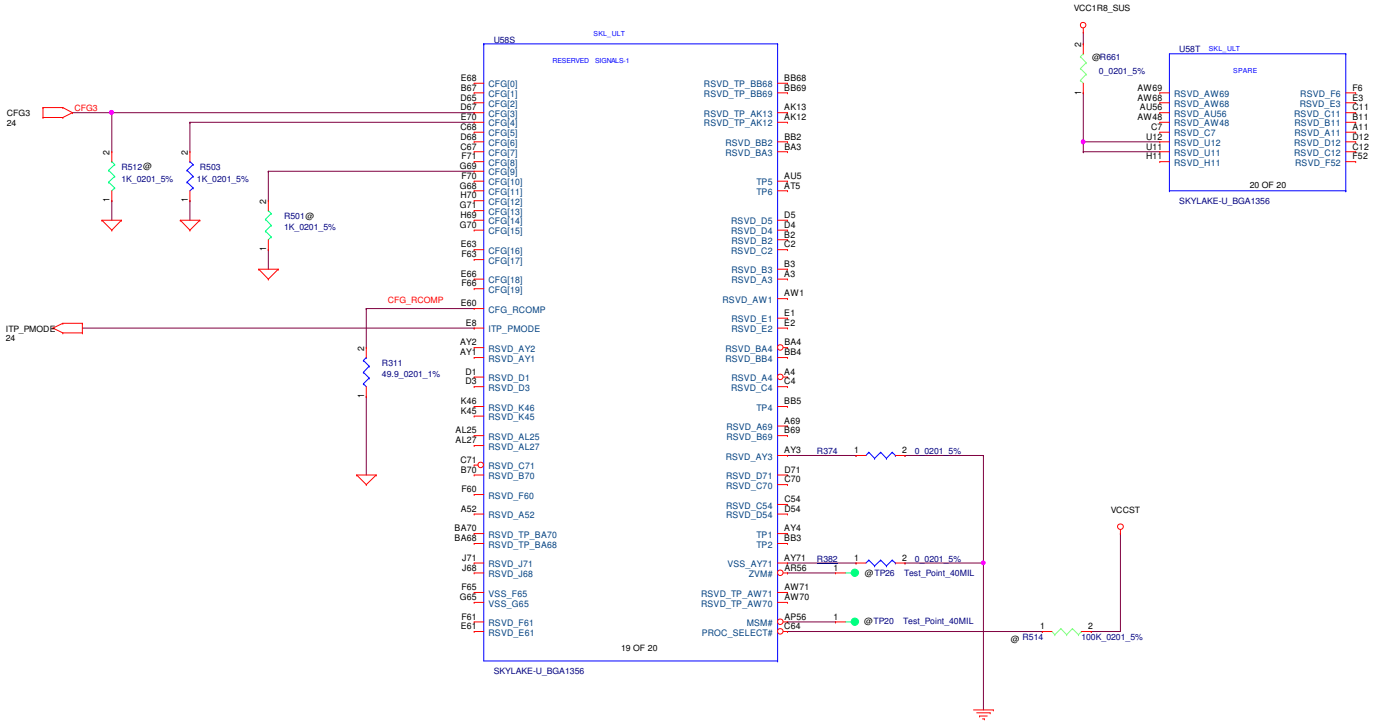
Title: CPU(15/16) : GND

Size	Document Number	Rev
Custom	COBAIN3	0.1

Date: Thursday, October 15, 2015 Sheet 17 of 97

TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted **1 : No Stall** **0 : Stall**
CFG4 : eDP Enable **1 : Disabled** **0 : Enabled**
CFG9 : SVID Bus Communication **1 : Enabled** **0 : Disabled**



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Issued Date	2012/05/02	Deciphered Date	2012/5/02

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Title: CPU(16/16) : CFG/RESERVED

Size	Document Number	Rev
Custom	COBAIN3	0.1

Date: Friday, October 16, 2015 Sheet 18 of 97

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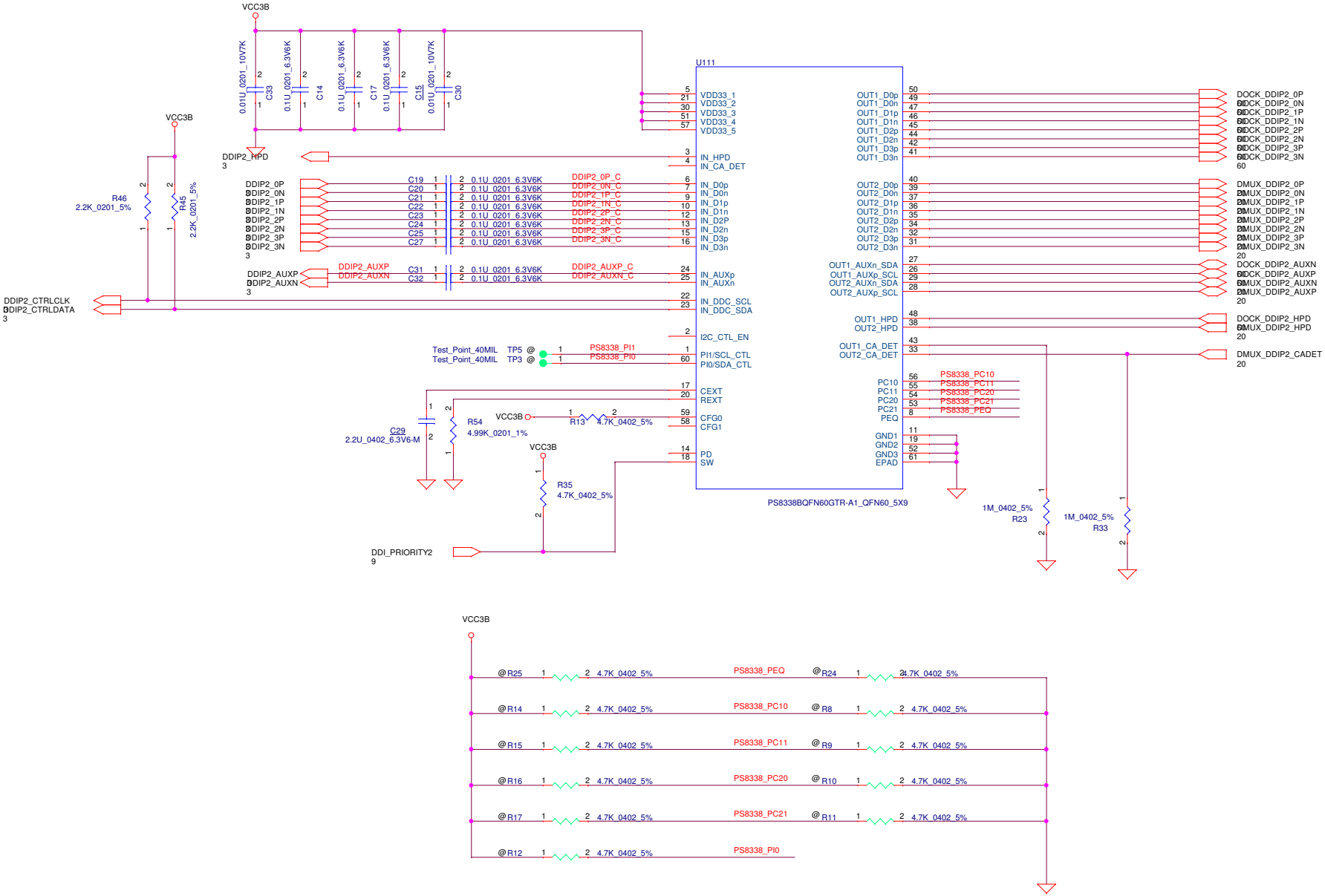

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Issued Date	2014/08/10	Deciphered Date	2015/08/10

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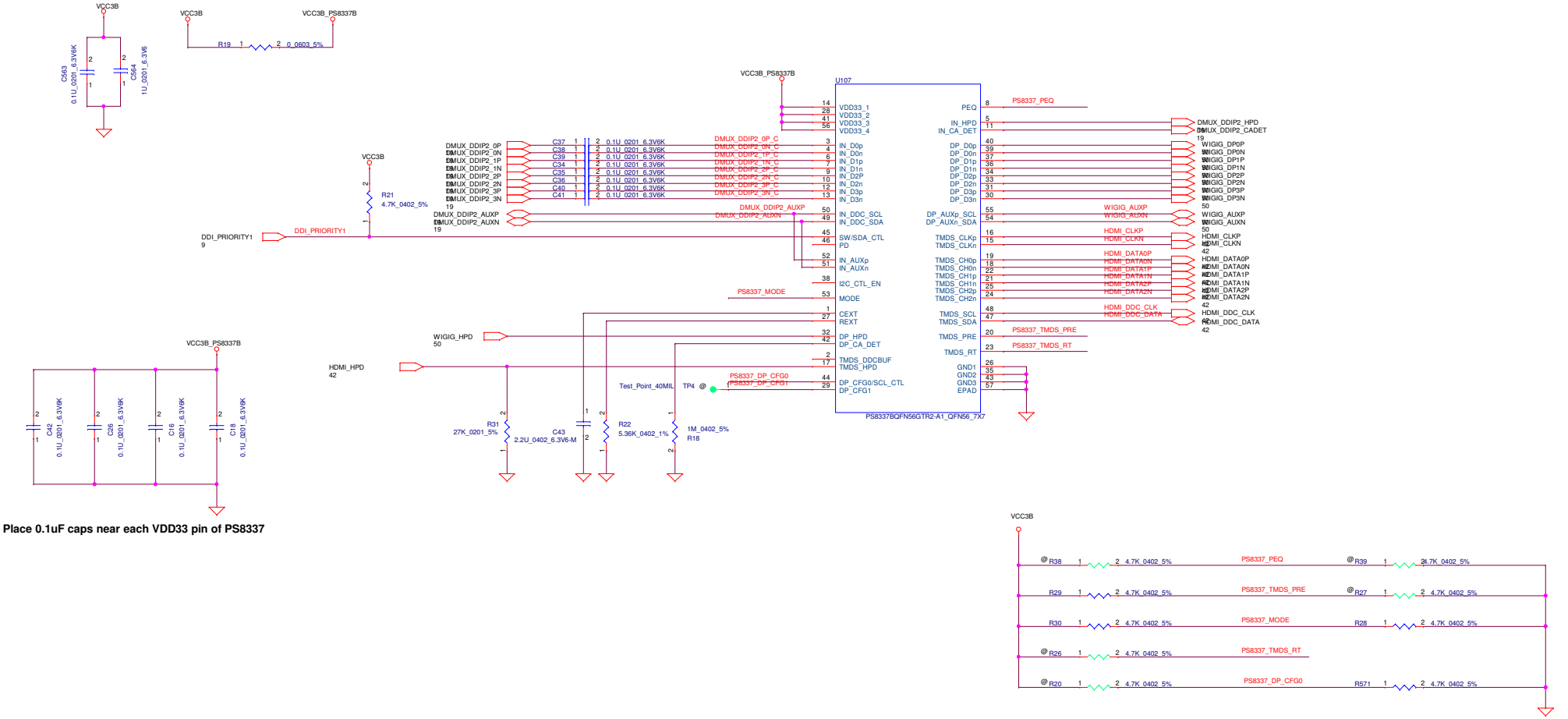
Title: DP SWITCH

Size	Document Number	Rev
Custom	COBAIN3	0.1

Date: Friday, October 16, 2015 Sheet 19 of 97



Place 0.1uF caps near each VDD33 pin of PS8337

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Issued Date	2014/08/10	Deciphered Date	2015/08/10

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Title: DP DEMUX

Size	Document Number	Rev
Custom	COBAIN3	0.1

Date: Friday, October 16, 2015 Sheet 20 of 97

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Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

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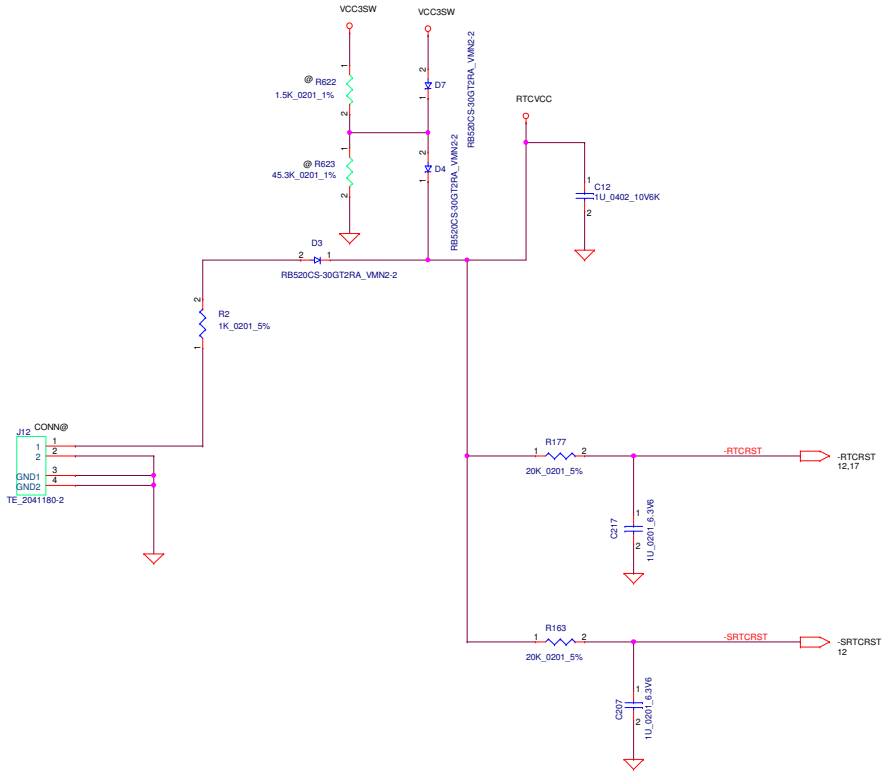
Title: HDMI RP

Size: B	Document Number: COBAIN3	Rev: 1.0
Date: Thursday, October 15, 2015	Sheet 21 of 97	

https://dr-bios.com



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: RTC BATTERY

Size	Document Number	Rev
Custom	COBA IN3	0.24

Date: Friday, October 16, 2015 Sheet 22 of 97

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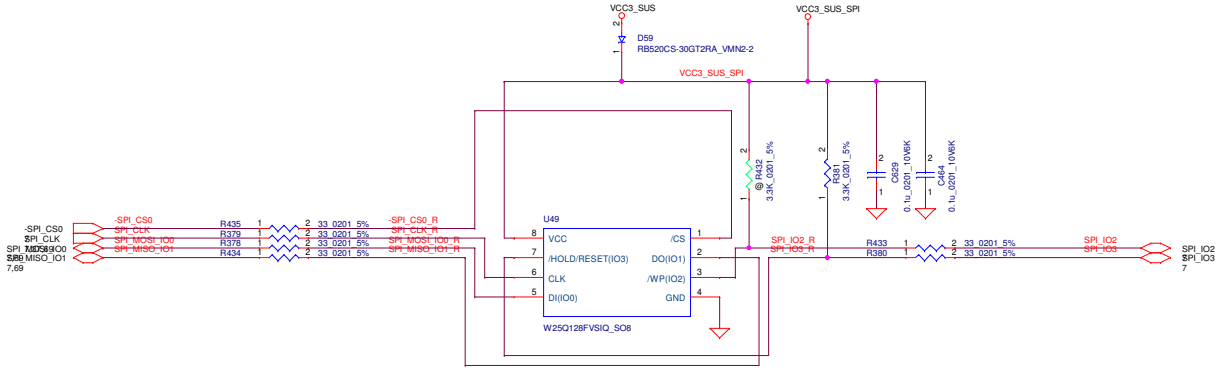

TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)					
1	VCC	D12.1	GND	GND	2
3	CS#	R322.2	R681.2	CLK	4
5	MISO	R694.2	R674.2	MOSI	6
7	(KEY)	N/A	N/A	(RESET)	8

U49 SPI ROM

vPro/non-vPro Model (16MB)	
WINBOND	W25Q128FVSIQ
MACRONIX	MX25L12875FM2I-10G

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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: *SPI FLASH*

Size	Document Number	Rev
Custom	*COBALN3*	0.1

Date: Friday, October 16, 2015 Sheet 23 of 97

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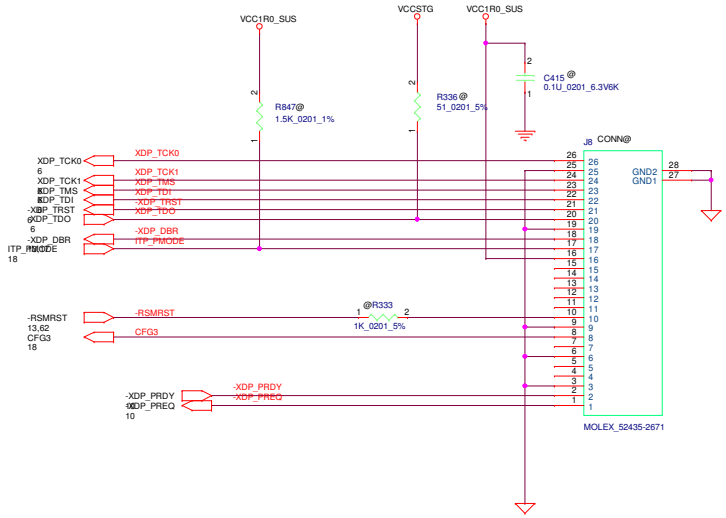

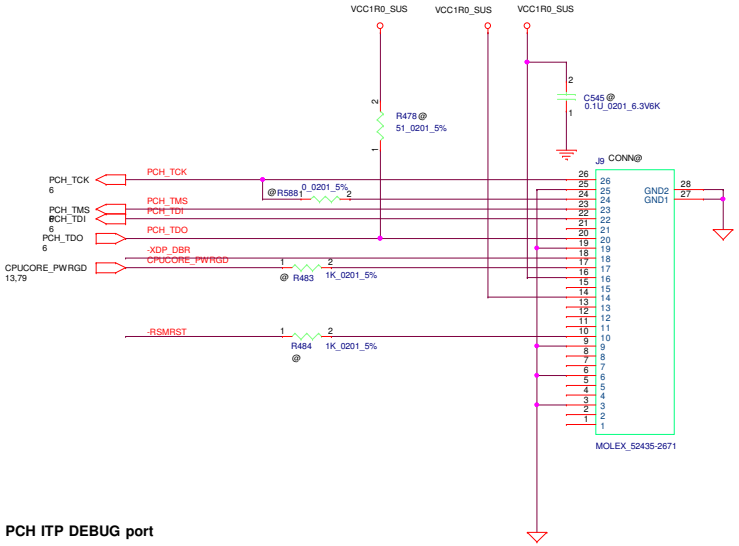

TABLE: PCH ITP DEBUG port

SIGNAL	REF DES	Planar only	BOX
TDO	R478 R523	ASM ASM	ASM ASM
TMS	R521	ASM	ASM
TDI	R535	ASM	ASM
TCK	R588 R538	ASM	ASM
CPUCORE_PWRGD	R483	ASM	ASM
-RSMRST	R484	ASM	ASM
CONNECTOR	J9	ASM	NO ASM

NOTE: APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV

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Title: XDP CONNECTOR

Size	Document Number	Rev
Custom	COBAIN3	0.1
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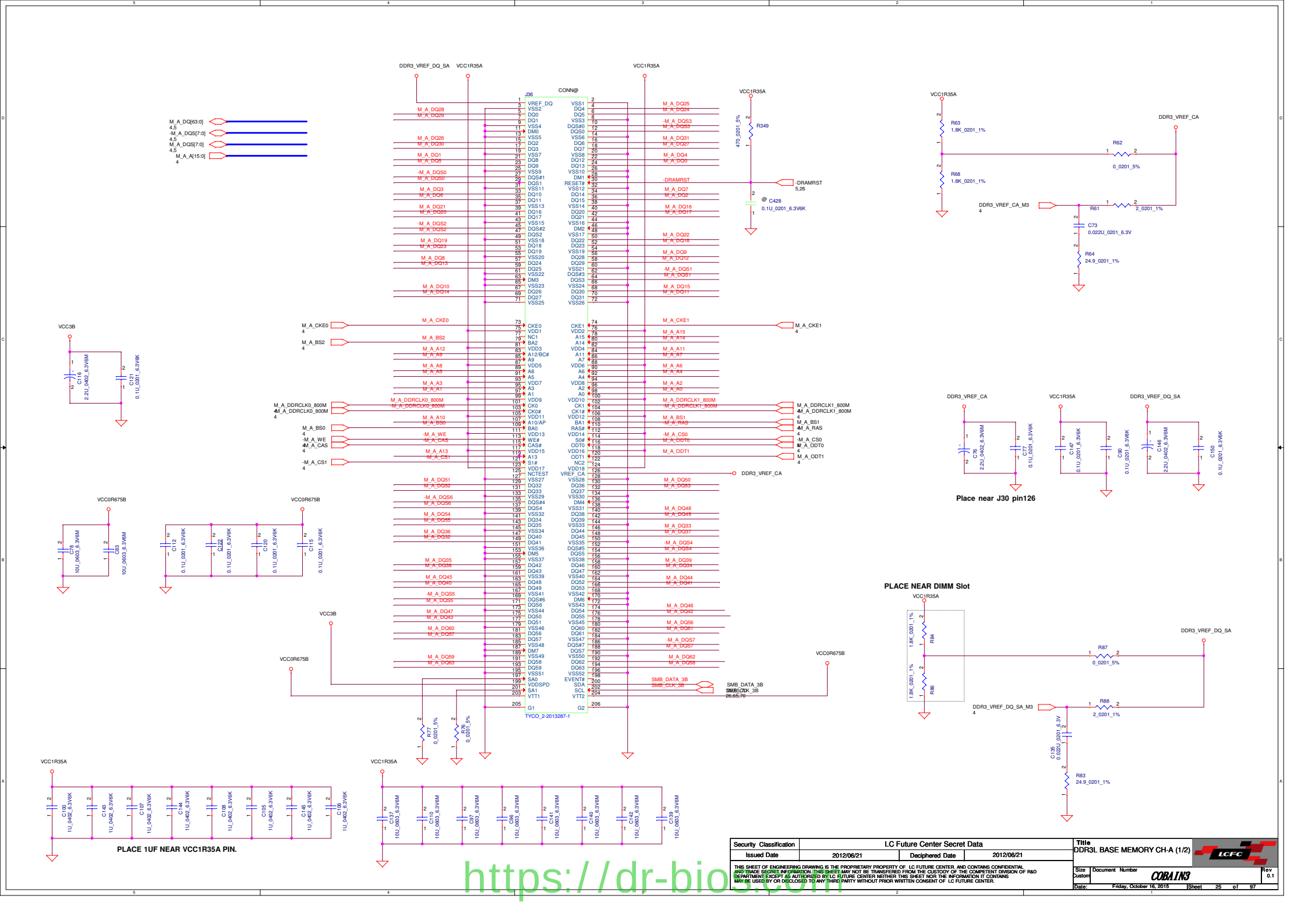
https://dr-bios.com



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Issued Date	2012/06/21	Deciphered Date	2012/06/21

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Title: DDR3L BASE MEMORY CH-A (1/2)

Size	Document Number	Rev
Custom	COBAIN3	0.1

Date: Friday, October 16, 2015 Sheet 25 of 97

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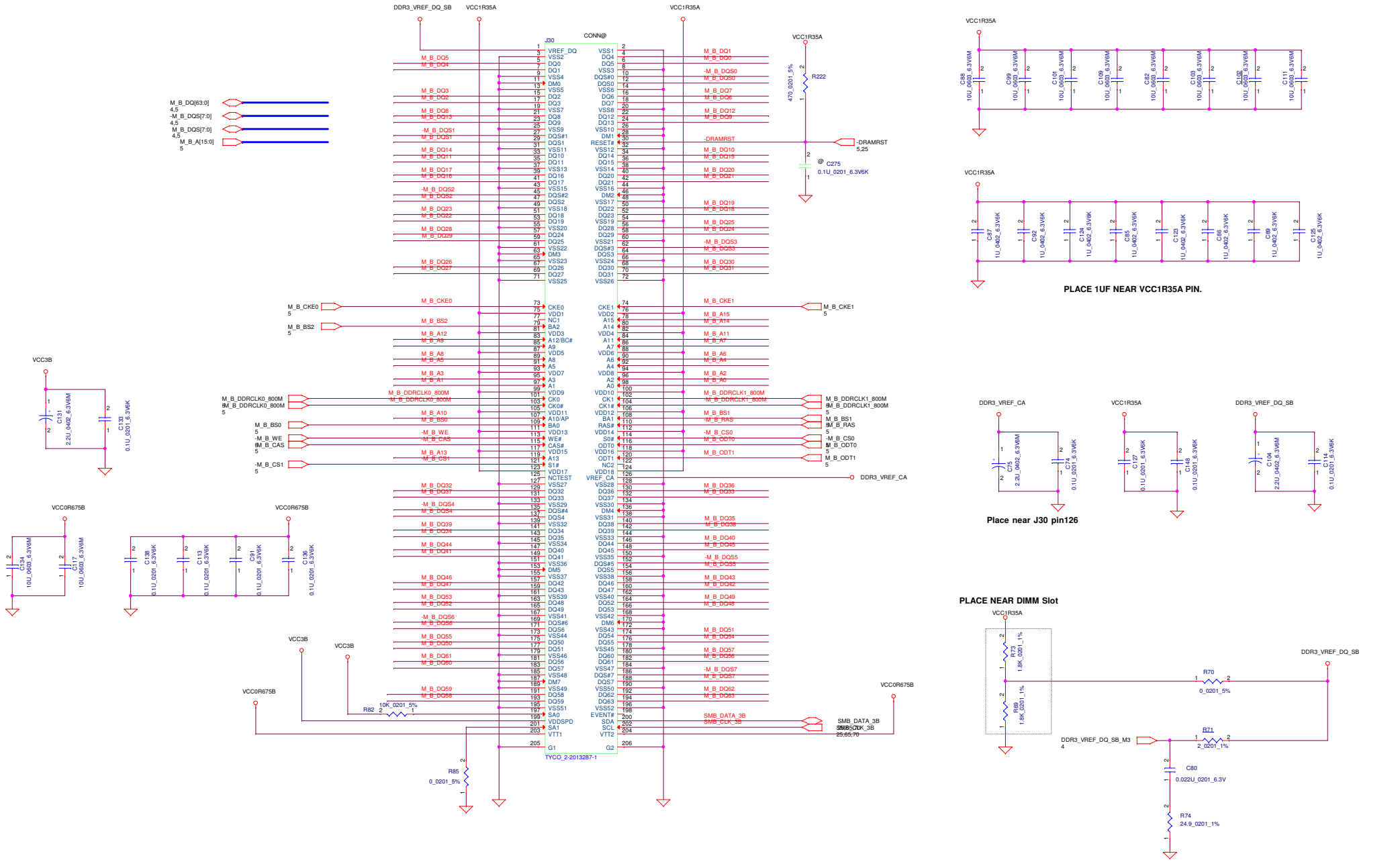

Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

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Title: DDR3L SO DIMM CHANNEL-B

Size	Document Number	Rev
Custom	COBAIN3	0.1
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Title: DDR3L DECOUPLING

Size: Custom	Document Number: COBAIN3	Rev: 0.1
Date: Thursday, October 15, 2015	Sheet 27 of 97	

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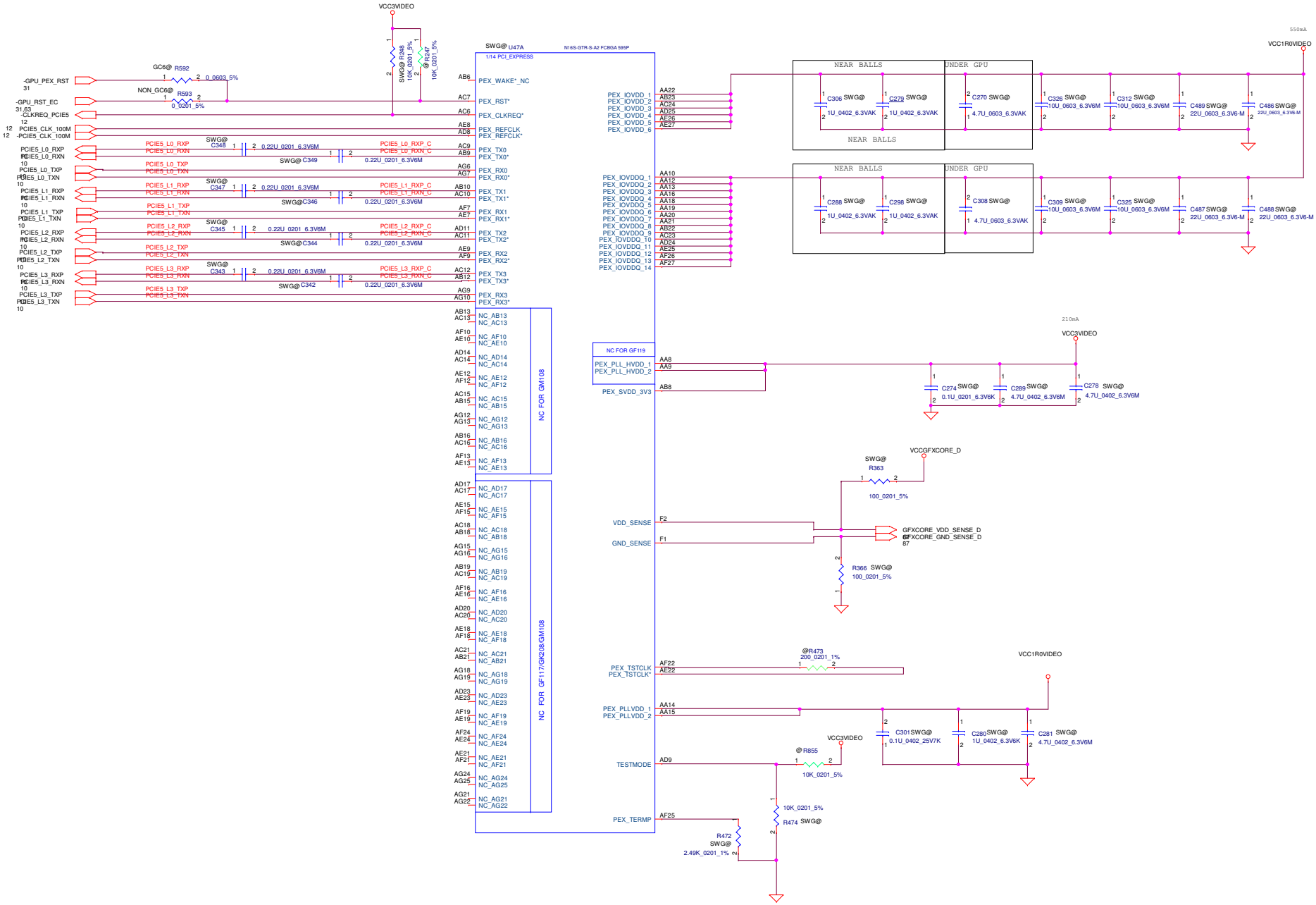

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Issued Date	2012/06/21	Deciphered Date	2012/06/21

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Title: N16S-GTR(1/6) PEG I/F

Size	Document Number	Rev
Custom	COBAIN3	0.1

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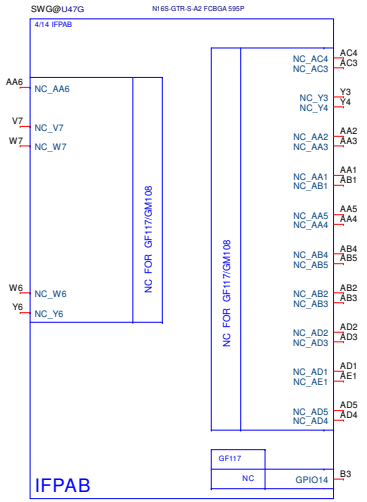

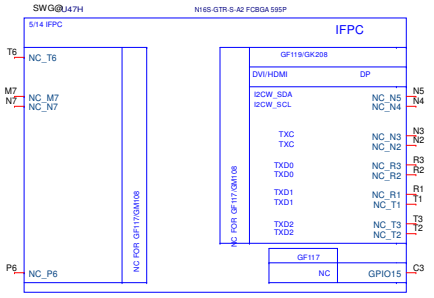

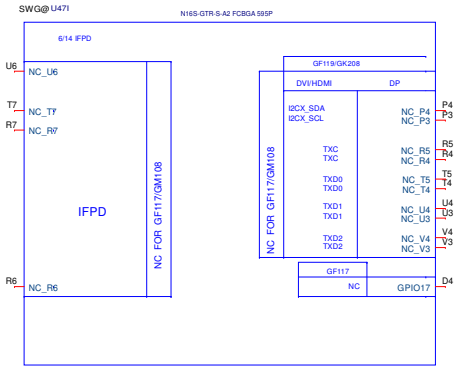

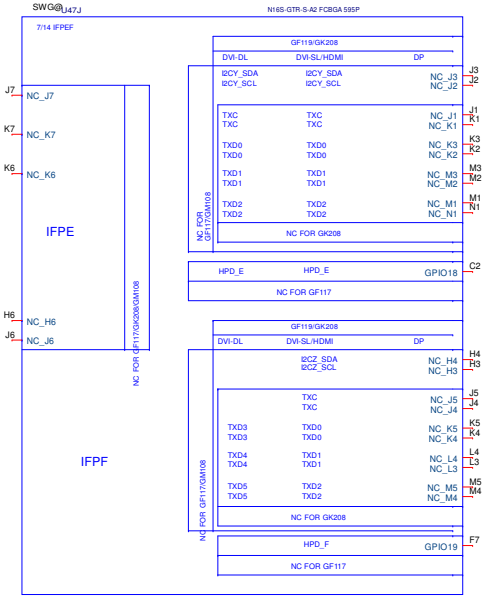

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Title: N16S-GTR(2/6) DIGITAL OUT I/F

Size	Document Number	Rev
Custom	COBAIN3	0.1

Date: Thursday, October 15, 2015 Sheet 29 of 97

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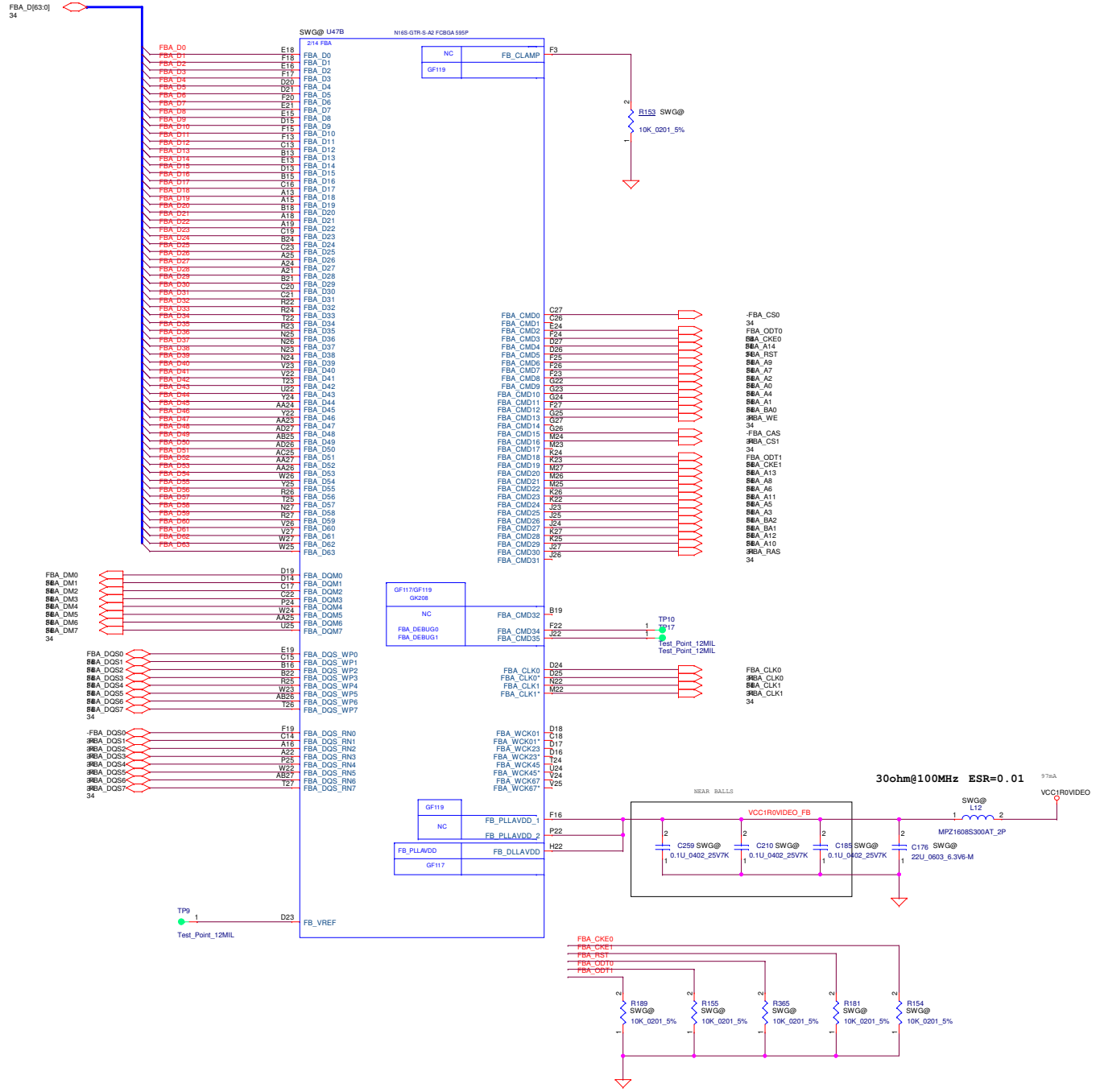

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Title: N16S-GTR(3/6) VRAM I/F

Size	Document Number	Rev
Custom	COBAIN3	0.1

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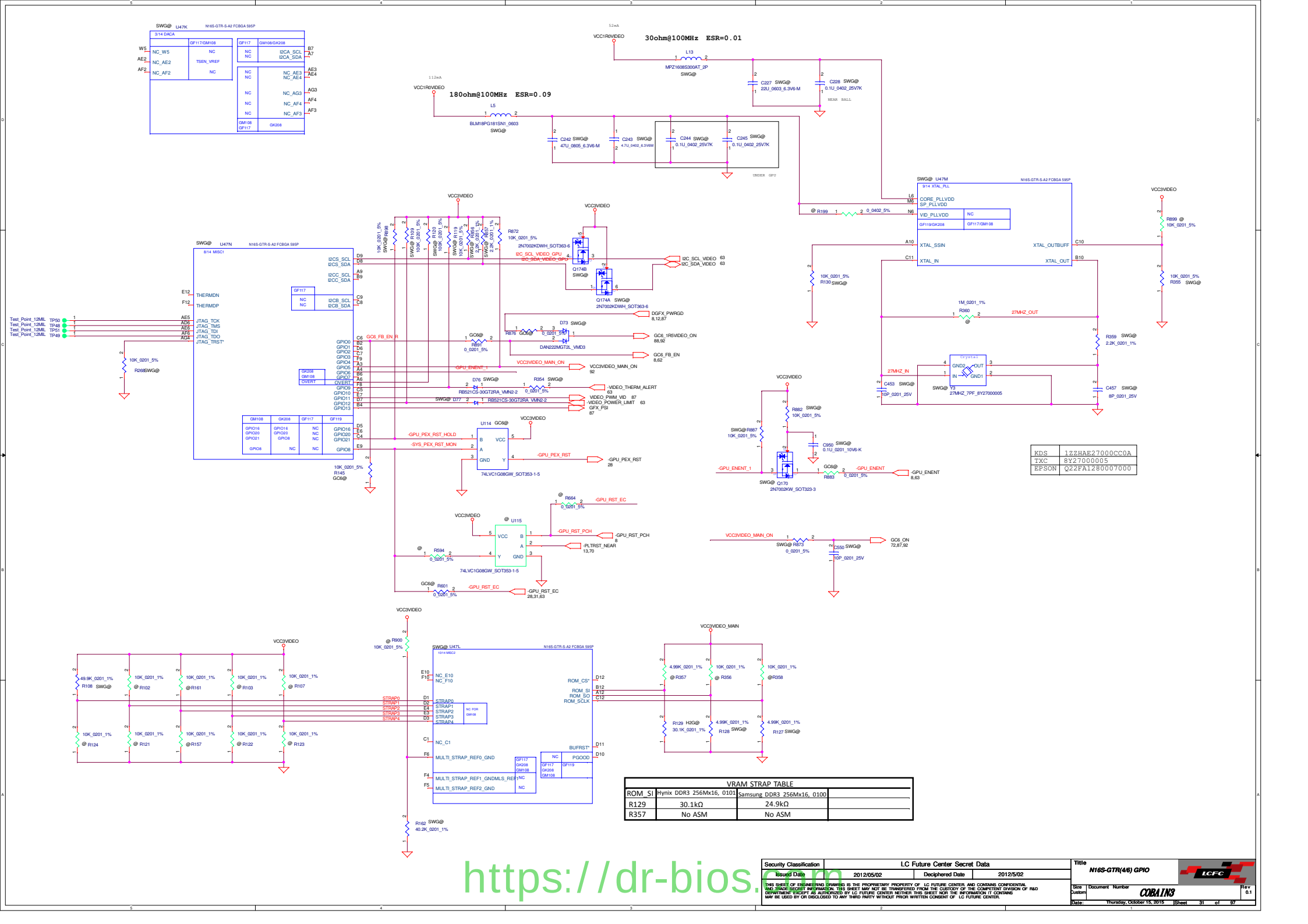

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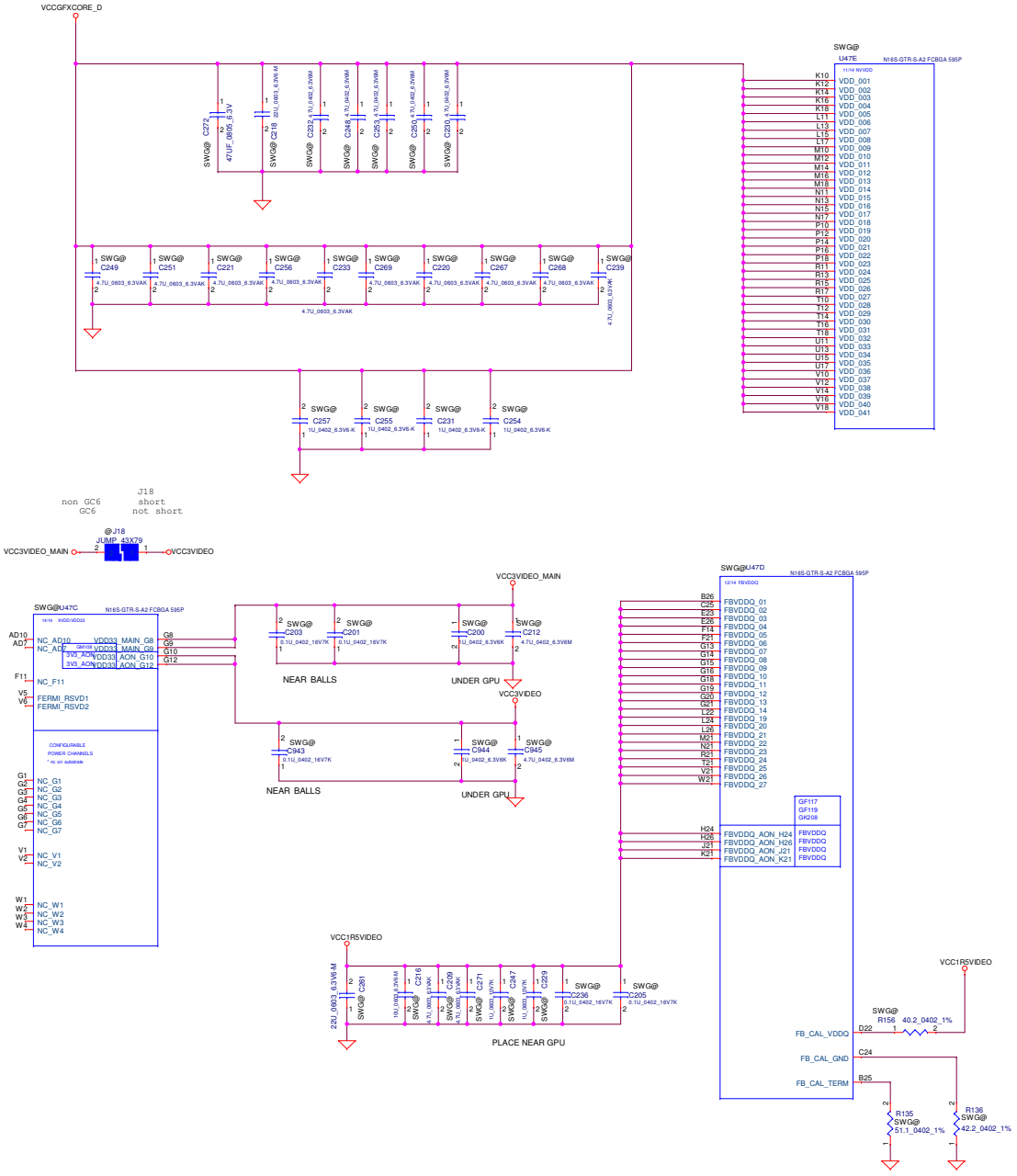

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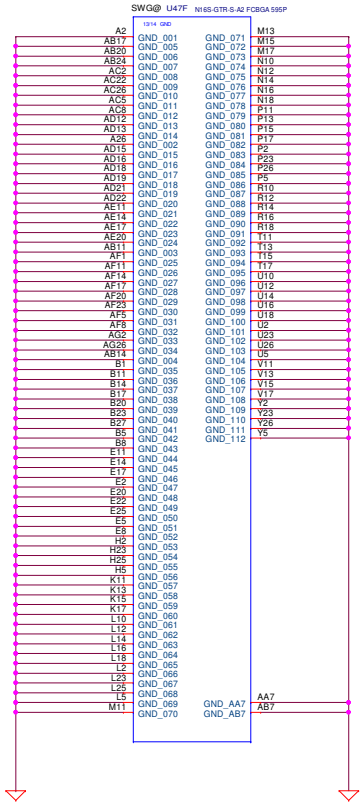
Title	N16S-GTR(5/6) POWER		
Size	Document Number		Rev
Custom	COBAIN3		0.1
Date:	Thursday, October 15, 2015	Sheet	32 of 97



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Title: N16S-GTR(6/6) GND

Size: Custom	Document Number: COBAIN3	Rev: 0.1
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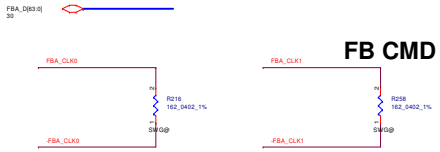
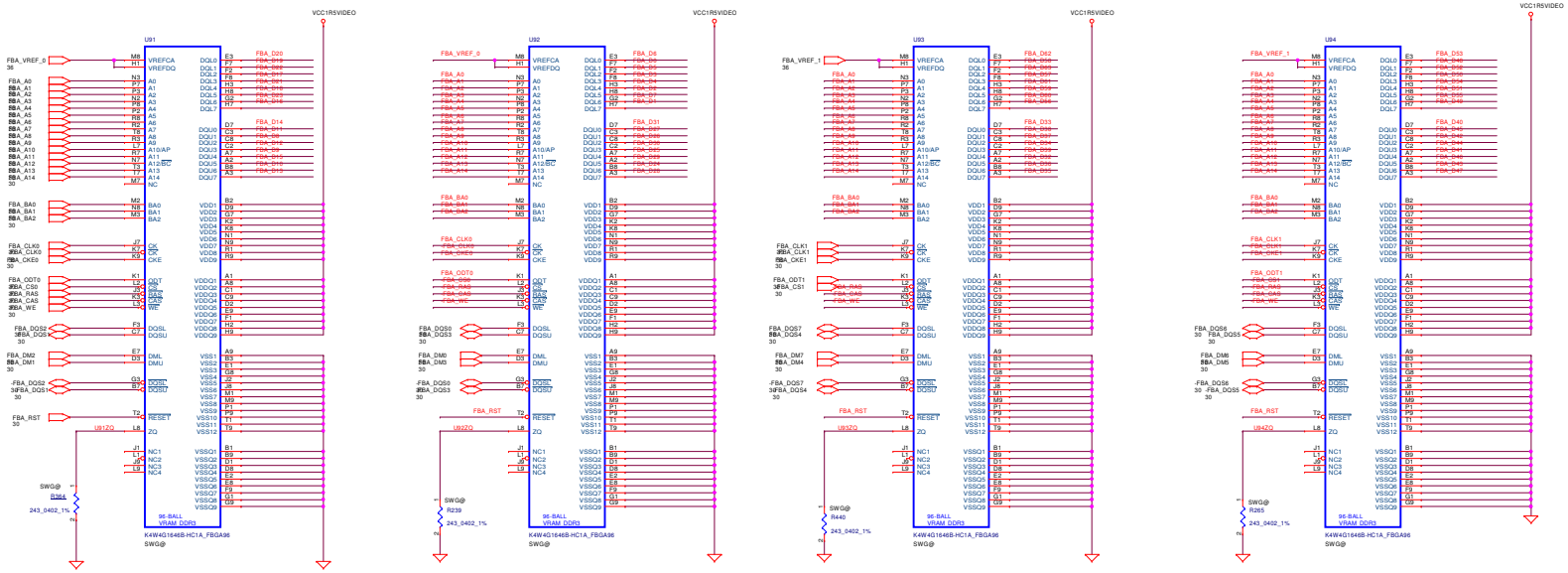
TABLE
DDR3 VIDEO MEMORY

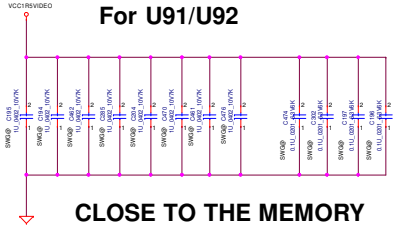
	Micron 2GBITS (128Mx16)	HYNIX 2GBITS(128Mx16)	SAMSUNG 2GBITS(128Mx16)	SAMSUNG 4GBITS(256Mx16)	HYNIX 4GBITS(256Mx16)
U91 U92 U93 U94				K4W4G1646E-BC1A	H5TC4G63CFR-N0C
BOM Structure				S2G@	H2G@

FB CMD mapping Mode D-N14x

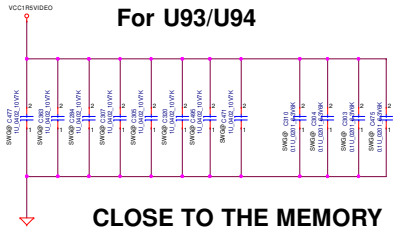




For U91/U92



CLOSE TO THE MEMORY



For U93/U94

CLOSE TO THE MEMORY

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Title: N16S-GTR VRAM CHANNEL-A

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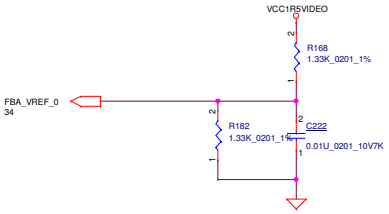

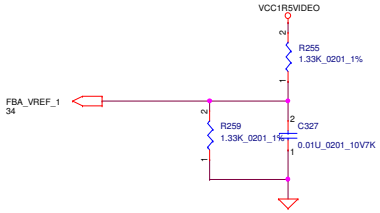

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Title: MEMORY TERMINATION

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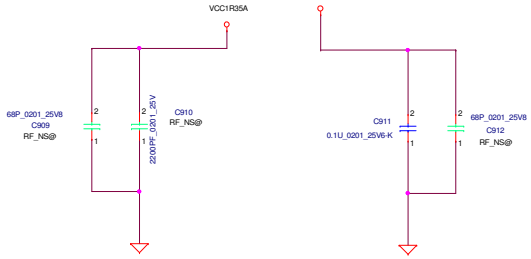

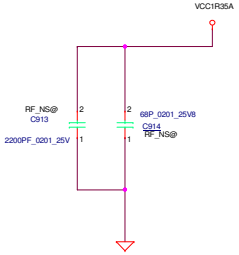

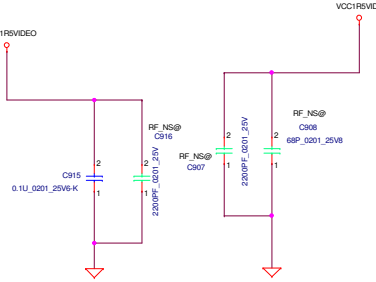

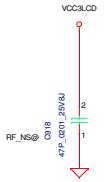

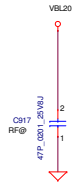

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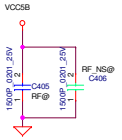

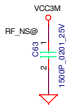

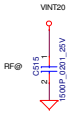

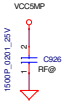

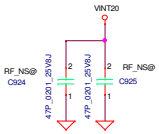

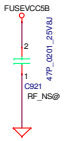

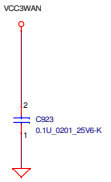

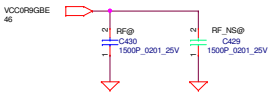

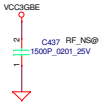

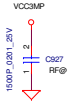

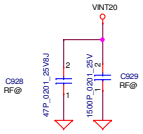

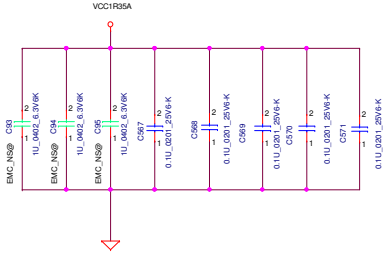

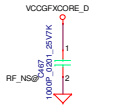

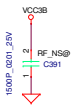

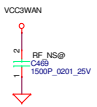

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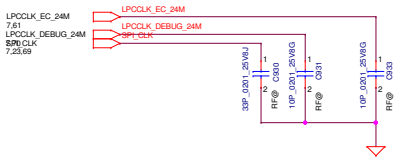

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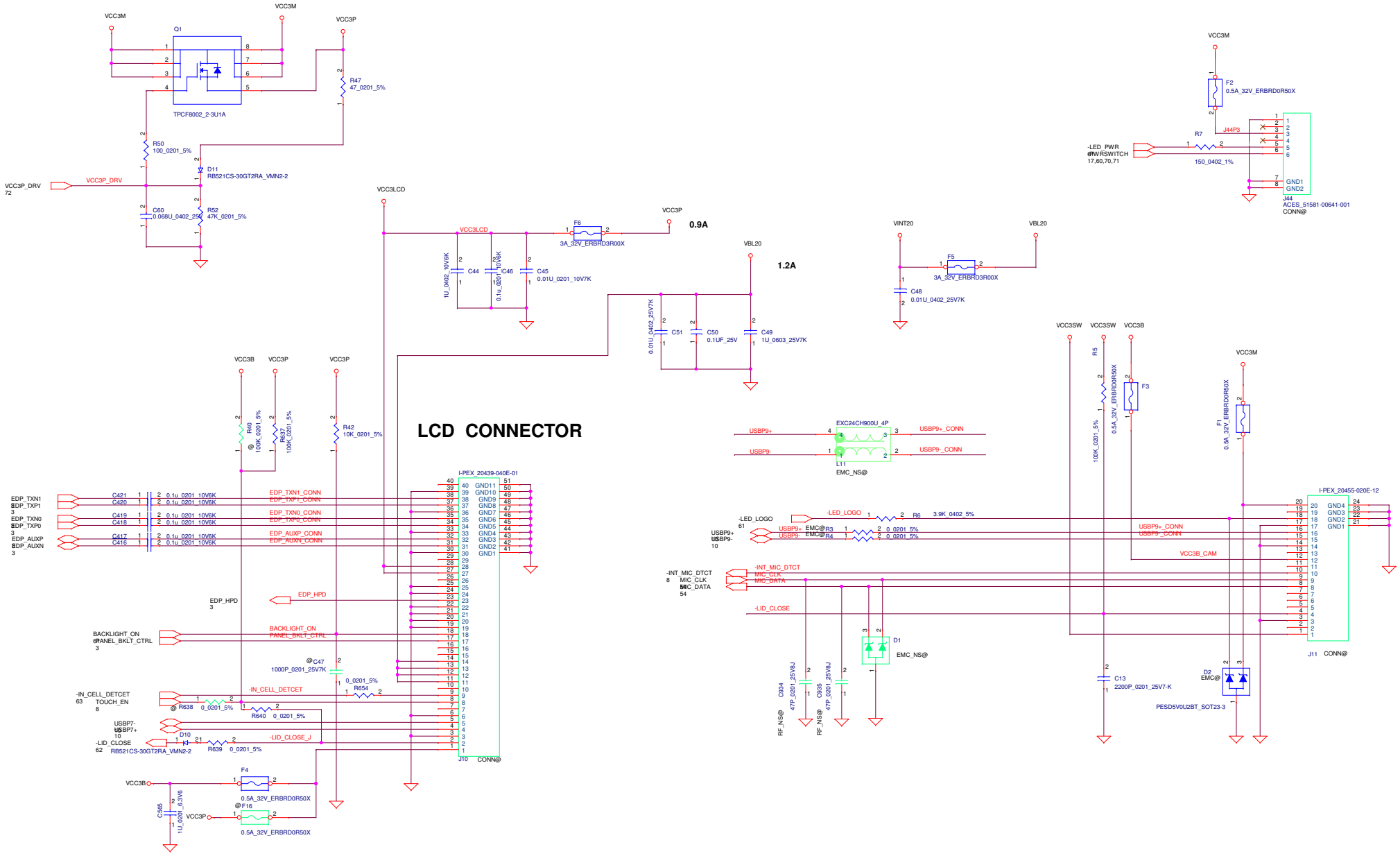

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Title	LCD CONNECTOR		
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Title: EXT CRT INTERFACE

LCFC

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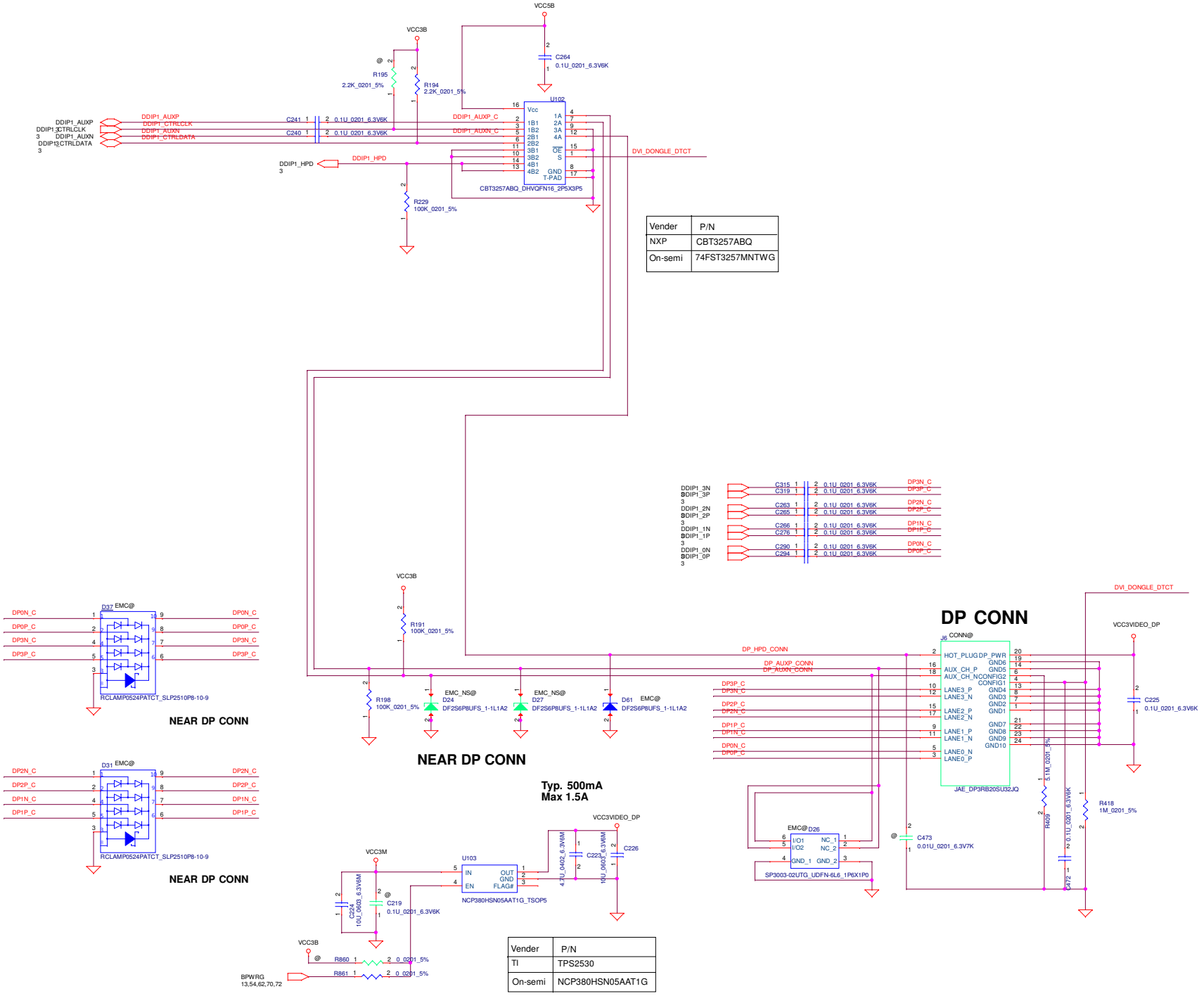

Vender	P/N
NXP	CBT3257ABQ
On-semi	74FST3257MNTWG

Vender	P/N
TI	TPS2530
On-semi	NCP380HSN05AAT1G

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Issued Date	2012/06/21	Deciphered Date	2012/06/21

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Title: DISPLAY PORT CONNECTOR

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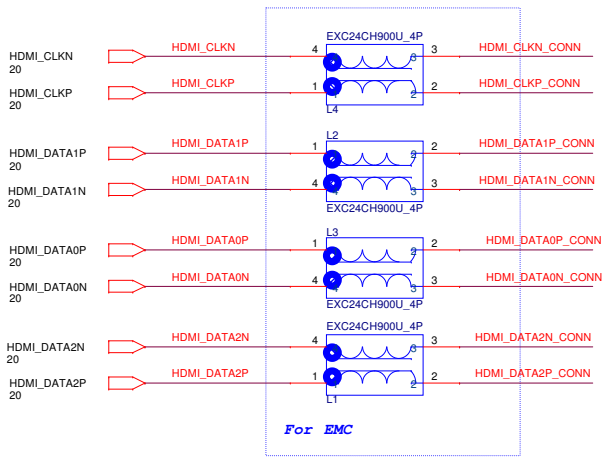
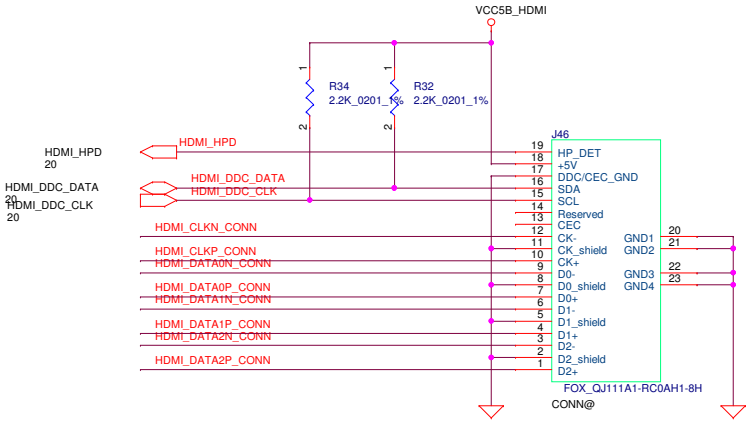
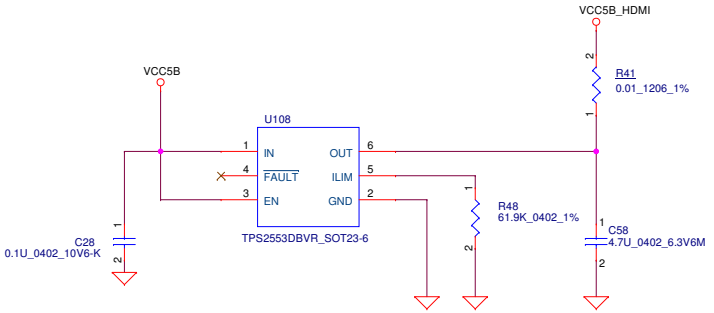
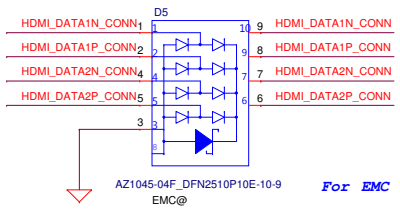
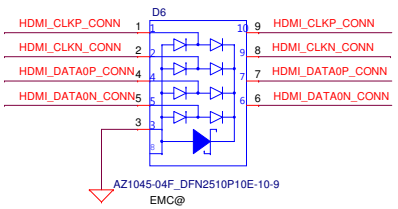


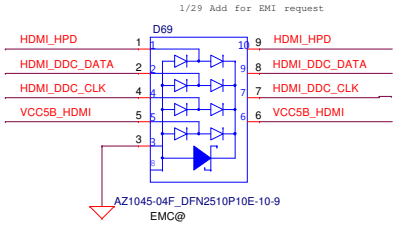




Close to J46







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Title	HDMI CONN		
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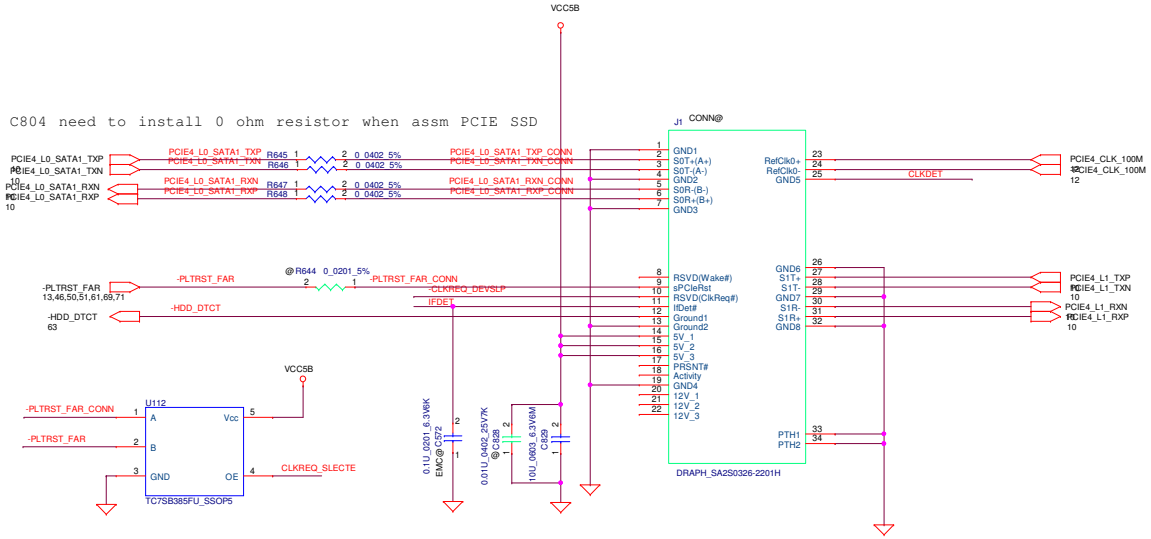
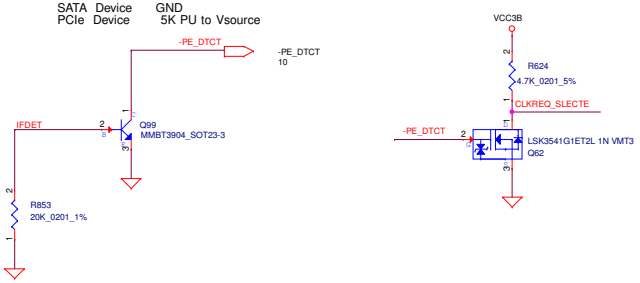
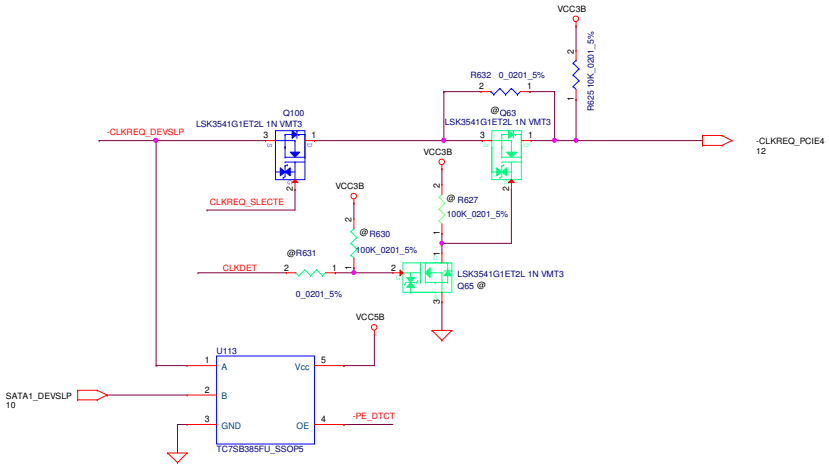
C803 and C804 need to install 0 ohm resistor when assm PCIE SSD



IFDET
SATA Device GND
PCIe Device 5K PU to Vsource





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Title: SATA HDD CONN

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Size	Document Number		Rev
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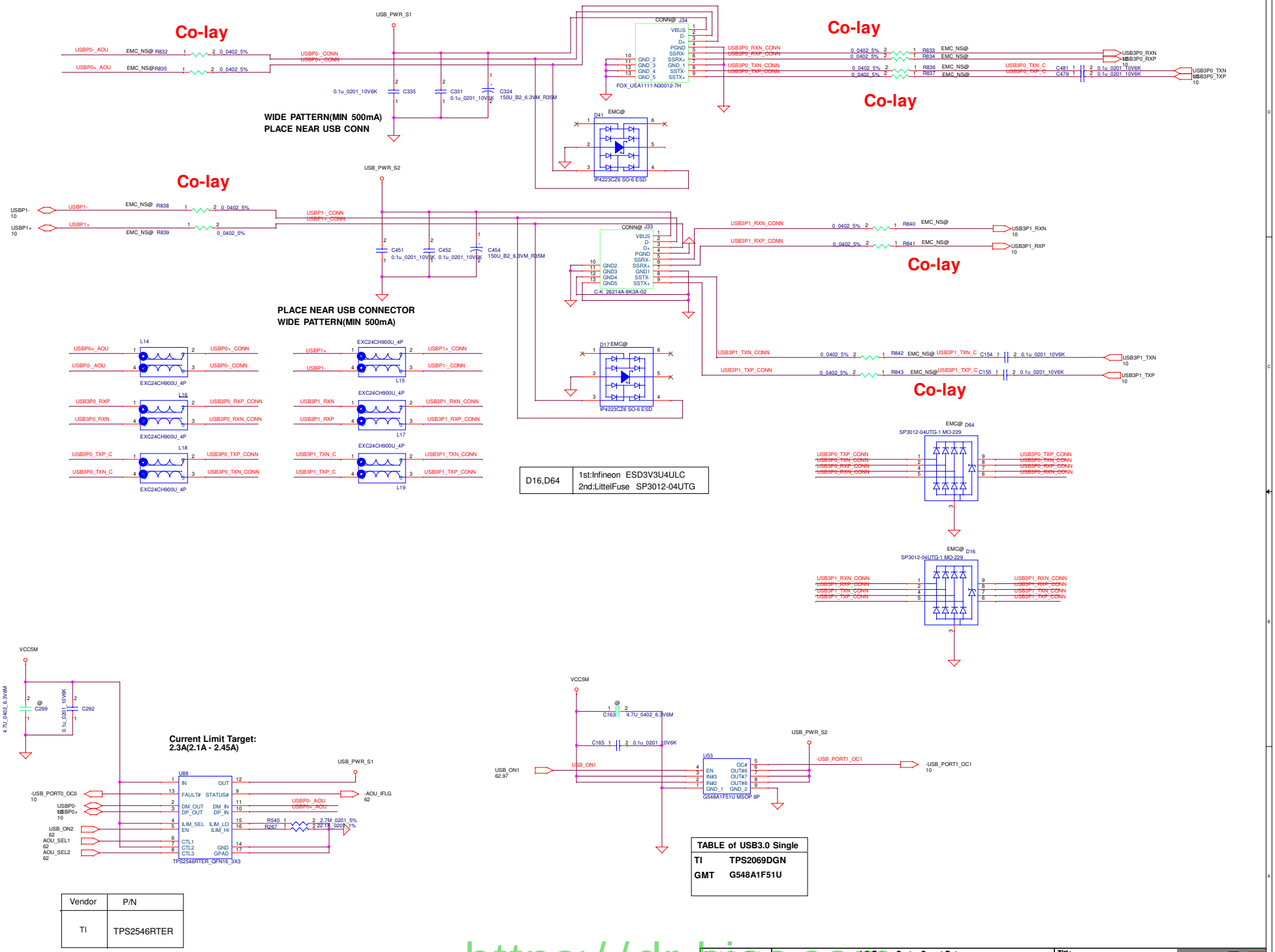

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Title: USB POWER/CONN

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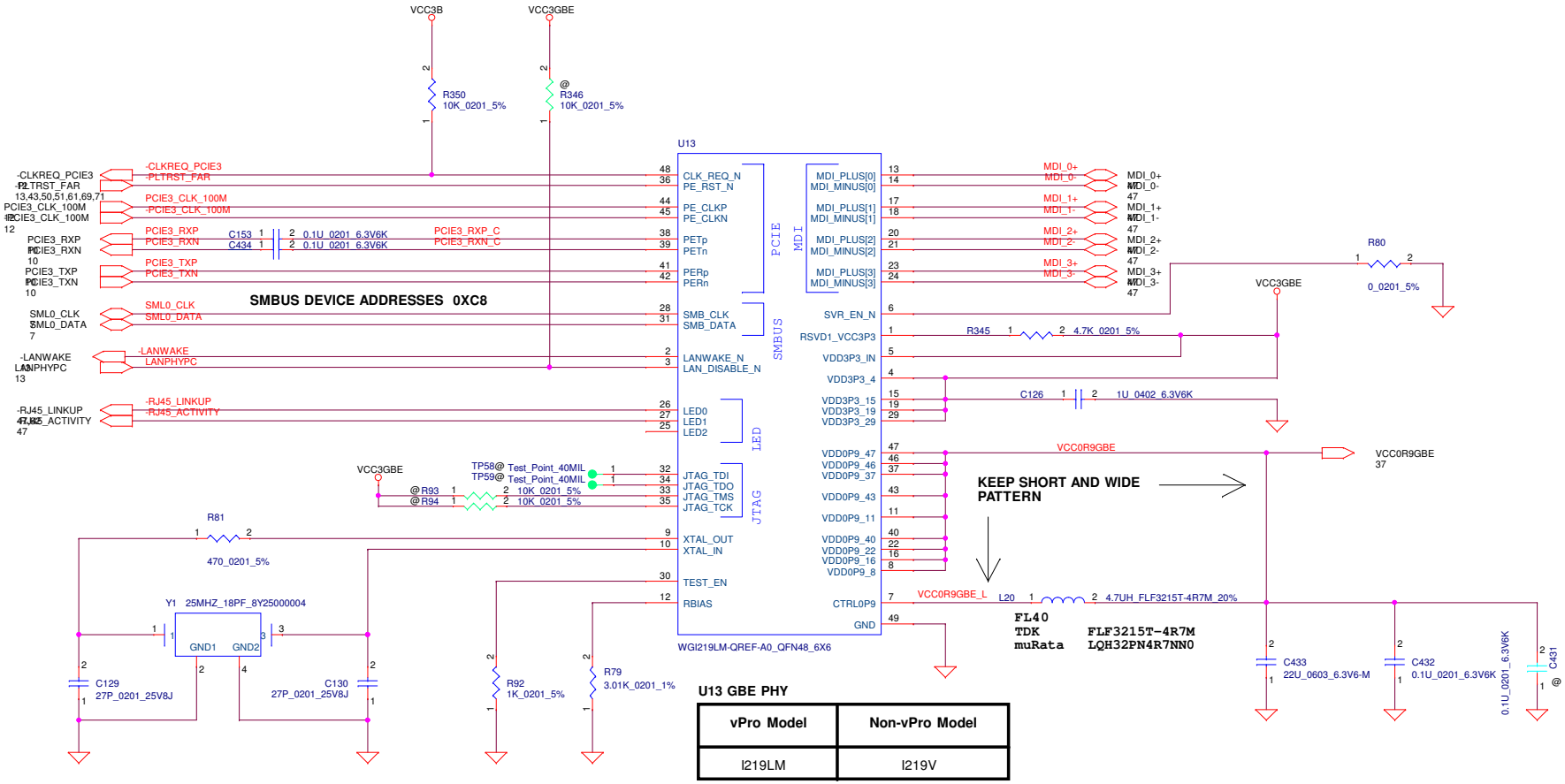
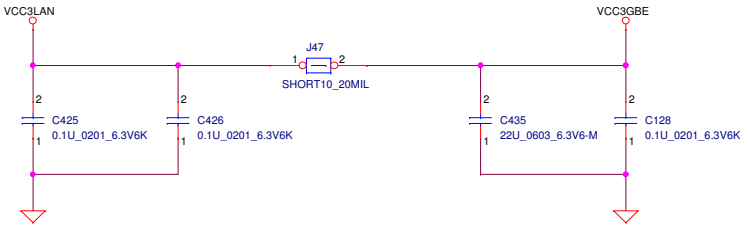


U13 GBE PHY

vPro Model	Non-vPro Model
I219LM	I219V

KDS 1ZZHAE25000CC0A
TXC 8Y25000004
EPSON Q22FA1280023800



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Issued Date	2012/05/01	Deciphered Date	2012/12/01

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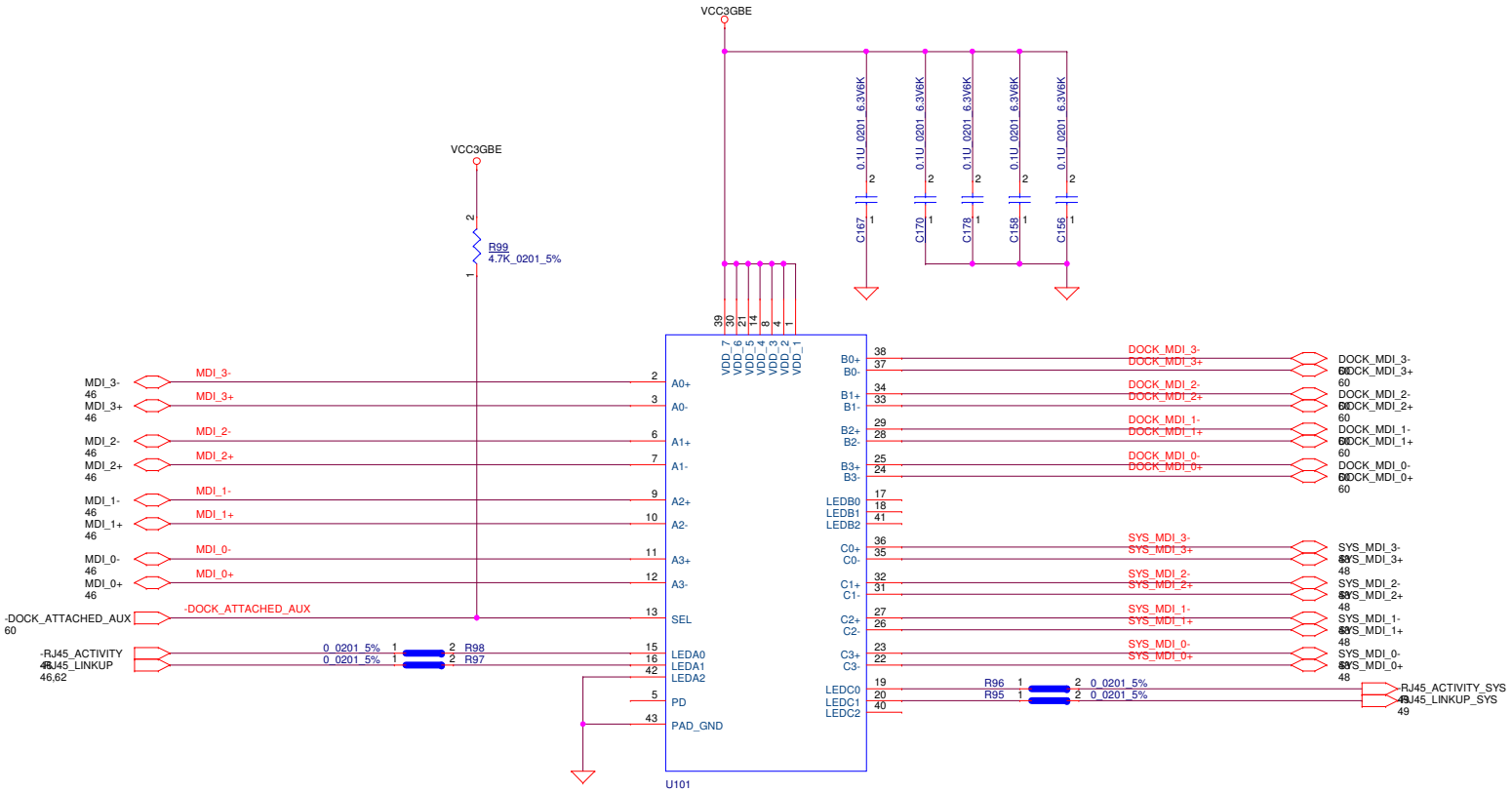
Title: GBE CLARKVILLE

Size	Document Number	Rev
Custom	COBAIN SWG	0.1

Date: Thursday, October 15, 2015 Sheet 46 of 97



U87

Vendor	P/N
Pericom ST micro Onsemi TI	PI3L720ZHE STMUX1800E NCN7201 TS3L501E

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Issued Date	2014/08/10	Deciphered Date	2015/08/10

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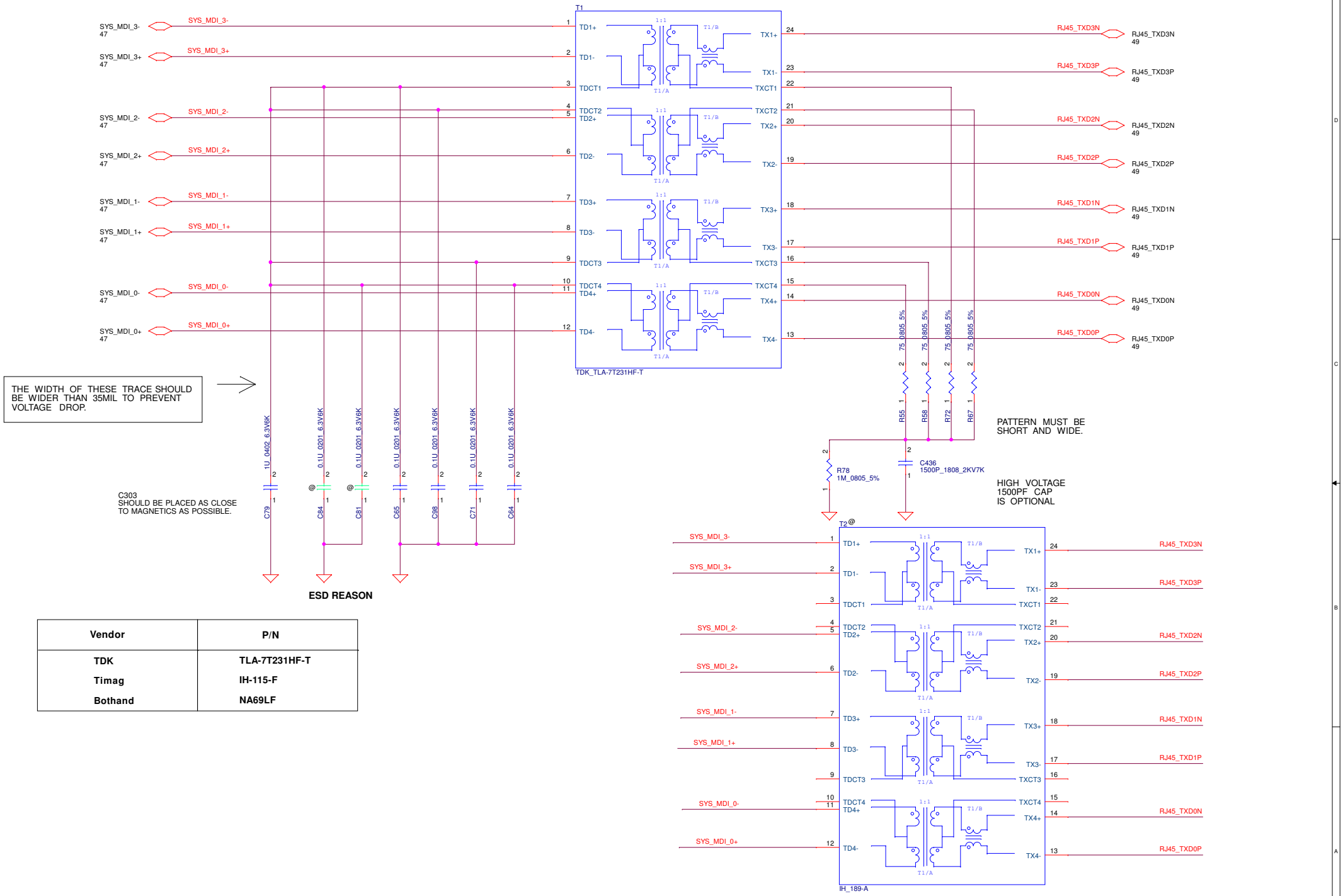
Title: GBE LAN SWITCH

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

Date: Thursday, October 15, 2015 Sheet 47 of 97



Vendor	P/N
TDK	TLA-7T231HF-T
Timag	IH-115-F
Bothand	NA69LF

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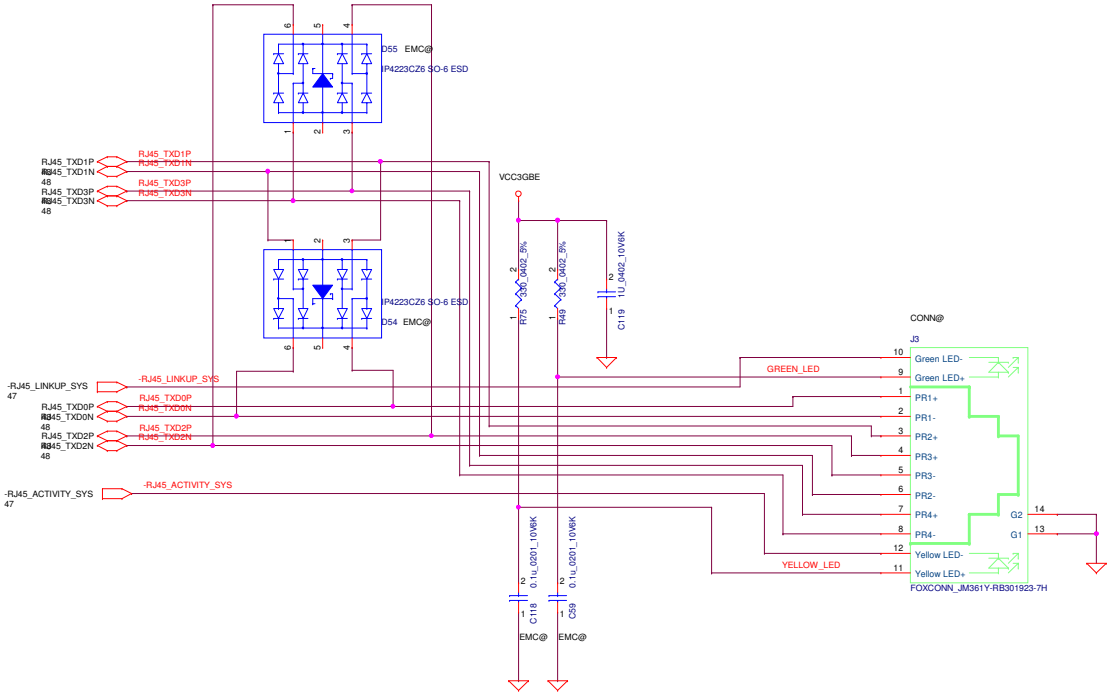
Title	GBE MAGNETICS		
Size: Custom	Document Number: COBAIN3		Rev: 0.1
Date: Thursday, October 15, 2015	Sheet 48 of 97		



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Issued Date	2012/05/02	Deciphered Date	2012/5/02

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Title: **RJ45 CONNECTOR**

Size	Document Number	Rev
Custom	COBAIN SWG	0.1
Date: Thursday, October 15, 2015	Sheet 49 of 97	

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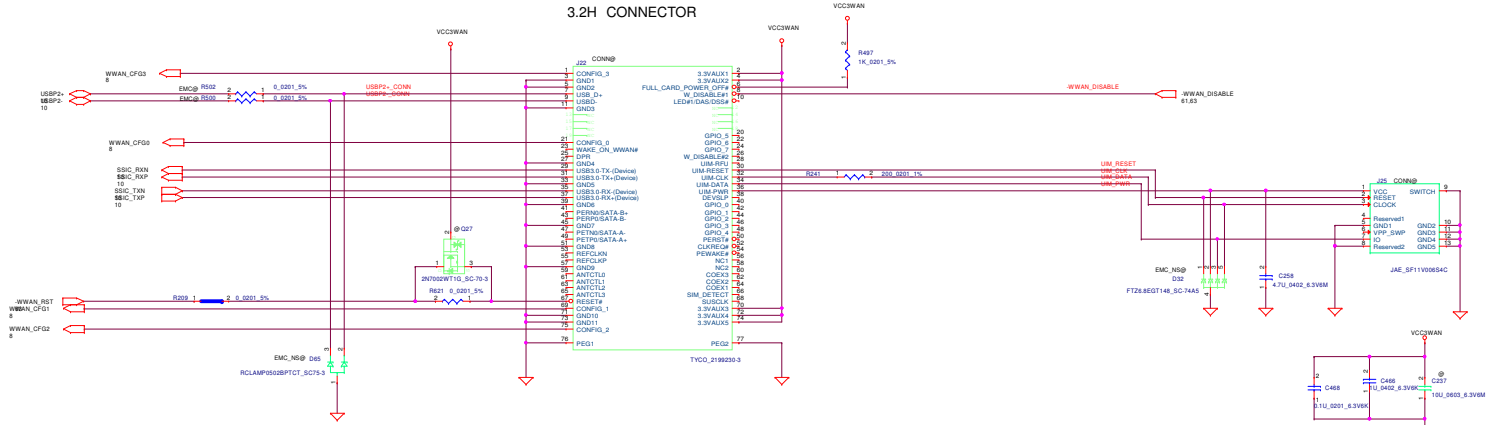
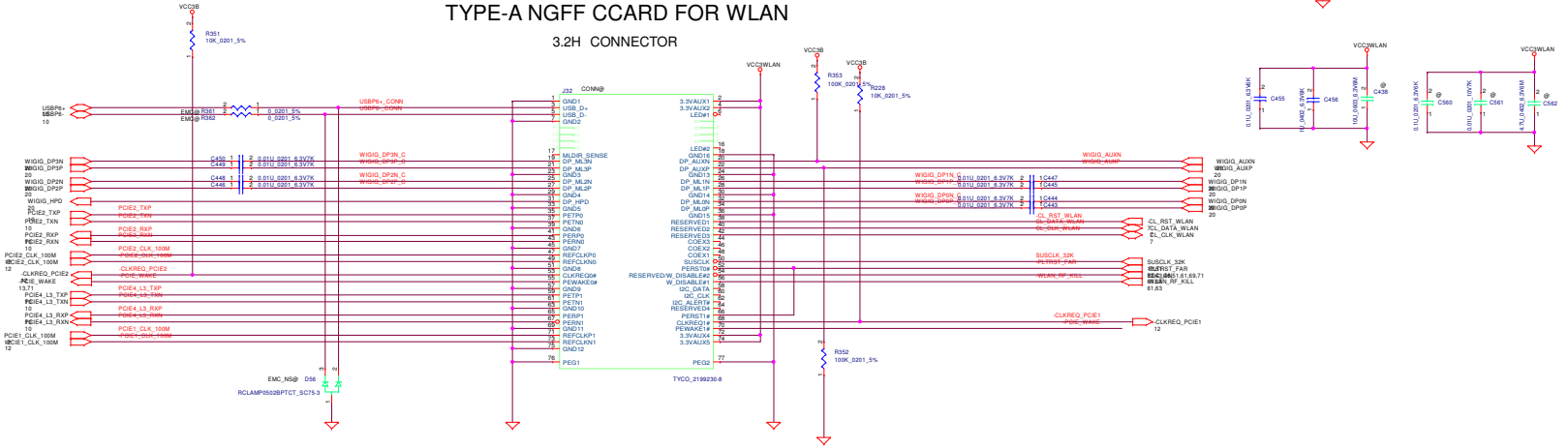
TYPE-B NGFF CCARD FOR WWAN/SSD

3.2H CONNECTOR



TYPE-A NGFF CCARD FOR WLAN

3.2H CONNECTOR



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Issued Date	2012/06/21	Deciphered Date	2012/06/21

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Title	PCIE MINI CARD SLOT		
Size	Document Number		Rev
D	COBAIN SRC		0.1
Date:	Monday, October 15, 2012	Sheet	50 of 97

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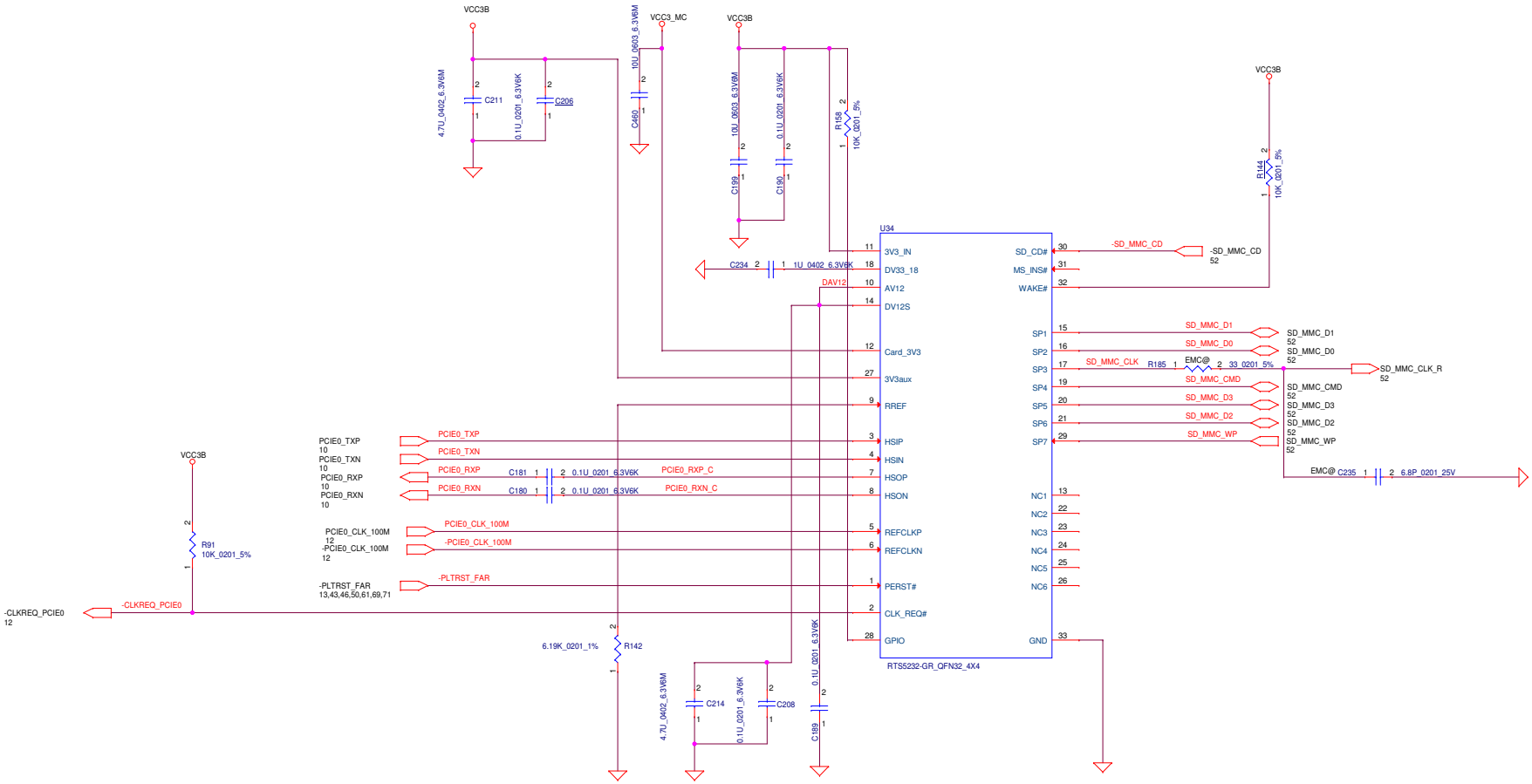

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Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/01	Deciphered Date	2012/12/01

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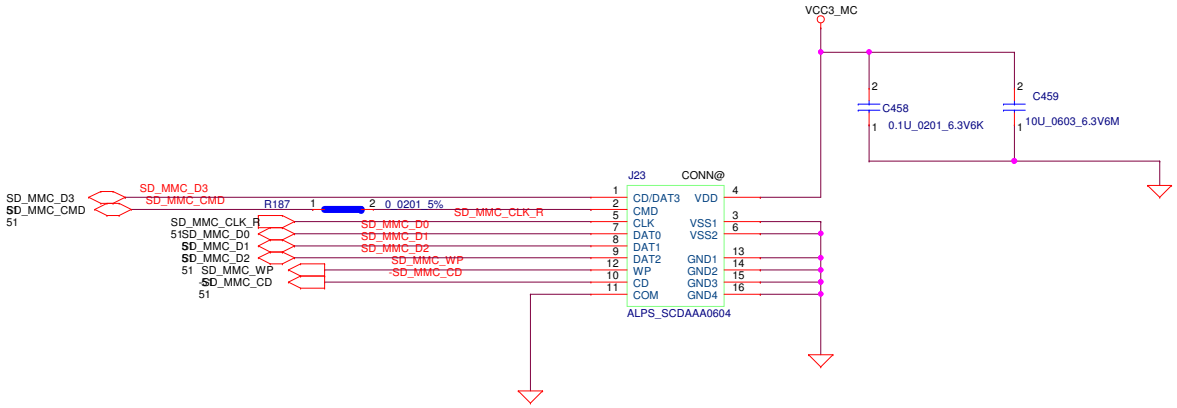
Title: MEDIA CARD CONTROLLER

Size	Document Number	Rev
Custom	COBAIN SWG	0.1

Date: Thursday, October 15, 2015 Sheet 51 of 97



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Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/01	Deciphered Date	2012/12/01

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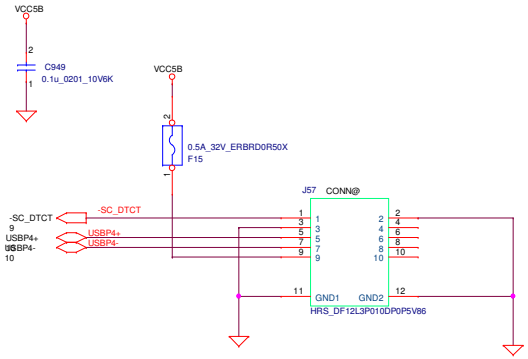
Title: MEDIA CARD INTERFACE

Size	Document Number	Rev
Custom	COBAIN3	0.1

Date: Thursday, October 15, 2015 Sheet 52 of 97



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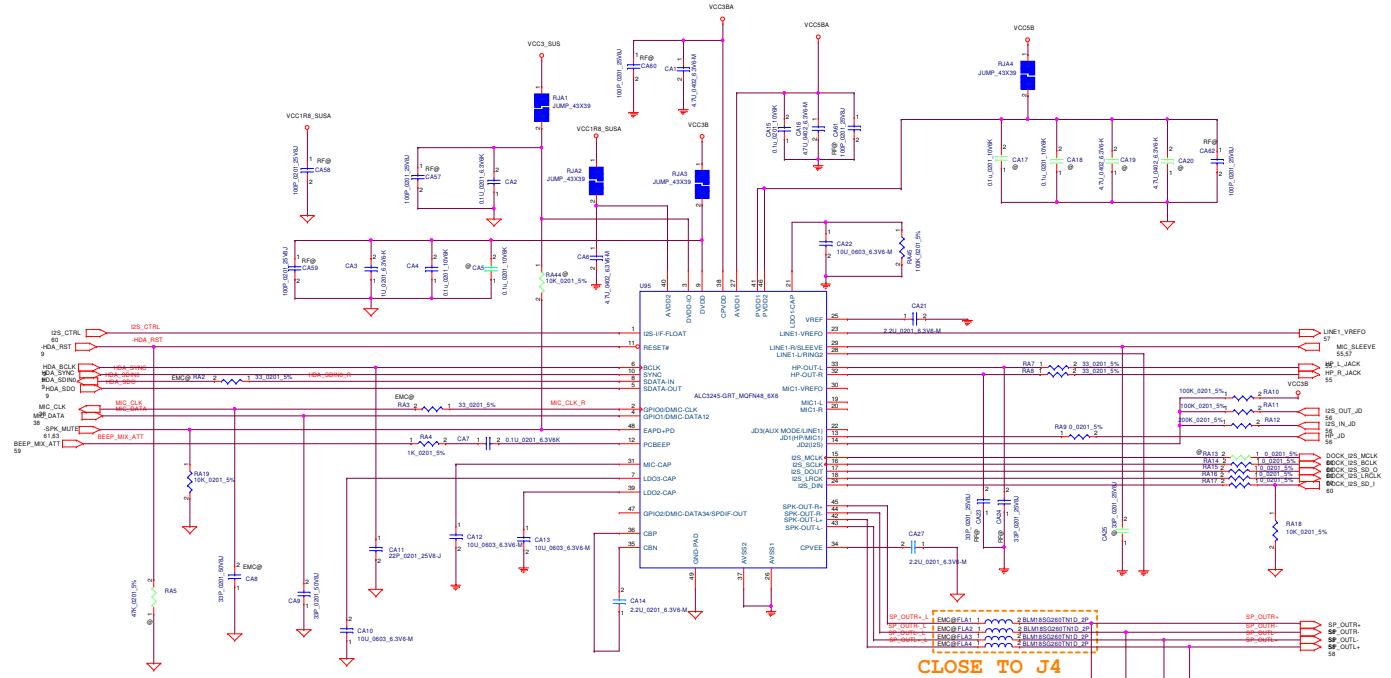
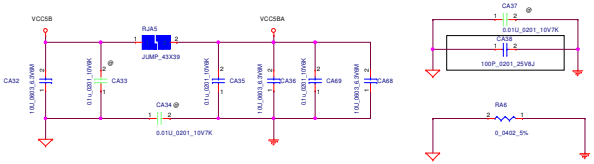
Title: SMART CARD I/F

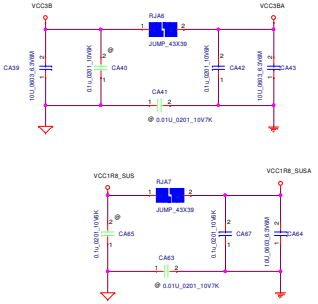
Size	Document Number	Rev
Custom	COBAIN3	0.1

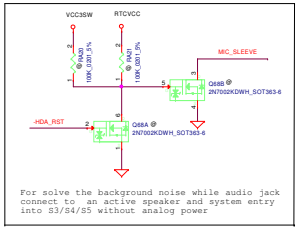
Date: Thursday, October 15, 2015 Sheet 53 of 97

https://dr-bios.com








For solve the background noise while audio jack connect to an active speaker and system entry into S3/S4/S5 without analog power

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Issued Date	2012/05/02	Deciphered Date	2012/5/02

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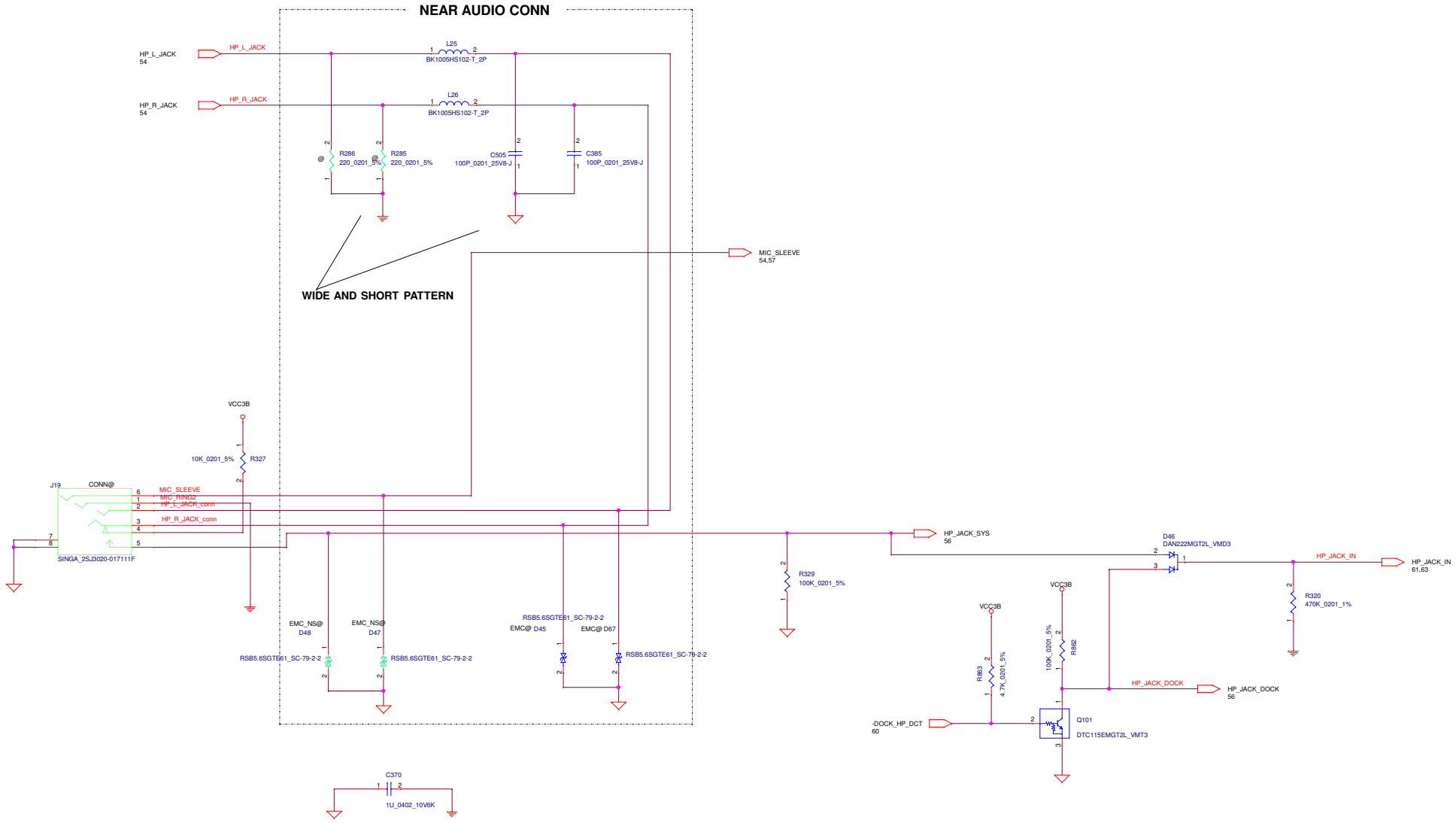
Title	Audio Codec		
Size	Document Number		Rev
D	Cobain9		0.1
Date:	Friday, October 19, 2012	Sheet	54 of 97

https://dr-bios.com



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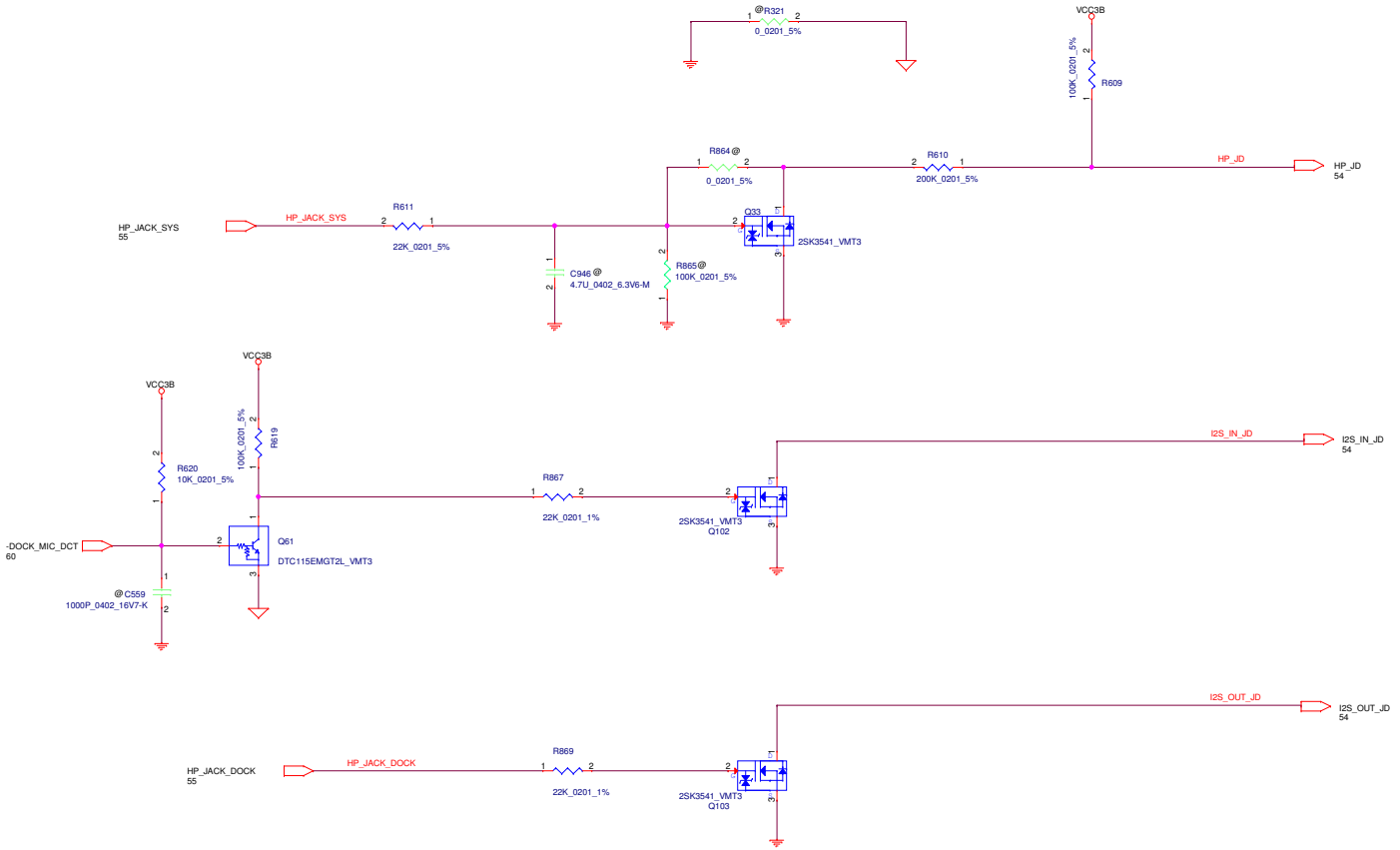
Title: AUDIO CONNECTOR

Size: Custom	Document Number: COBAIN3	Rev: 0.1
Date: Thursday, October 15, 2015	Sheet 55 of 97	

https://dr-bios.com



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Title: AUDIO JACK SENSE

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COBAIN3

Date: Thursday, October 15, 2015 Sheet 56 of 97

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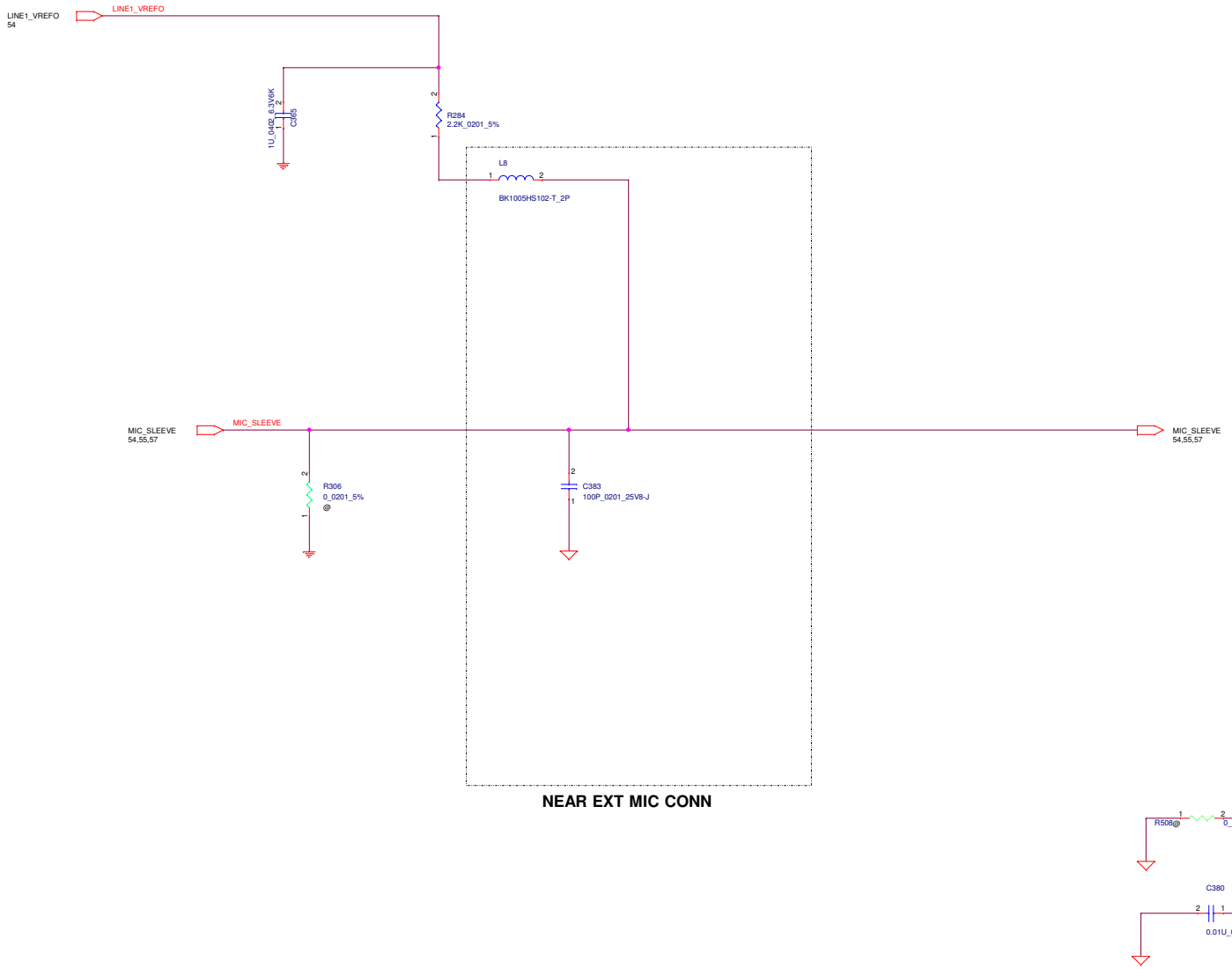

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Title: AUDIO EXT MIC I/F

Size: Custom	Document Number: COBAIN SWG	Rev: 0.1
Date: Thursday, October 15, 2015	Sheet 57 of 97	

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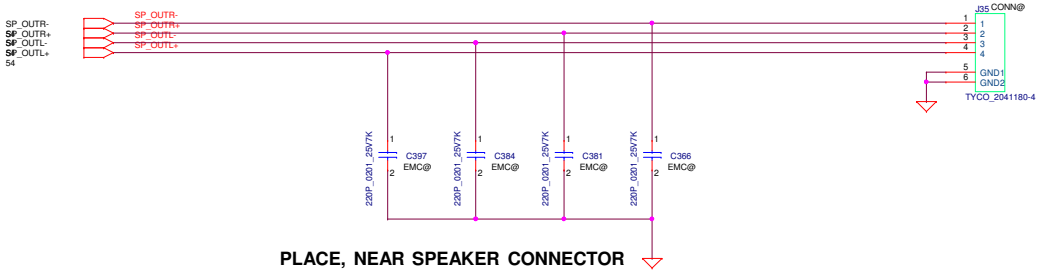

PLACE, NEAR SPEAKER CONNECTOR

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Title: **AUDIO SPEAKER**

Size: Custom	Document Number: COBAIN SWG	Rev: 0.1
Date: Thursday, October 15, 2015	Sheet 58 of 97	

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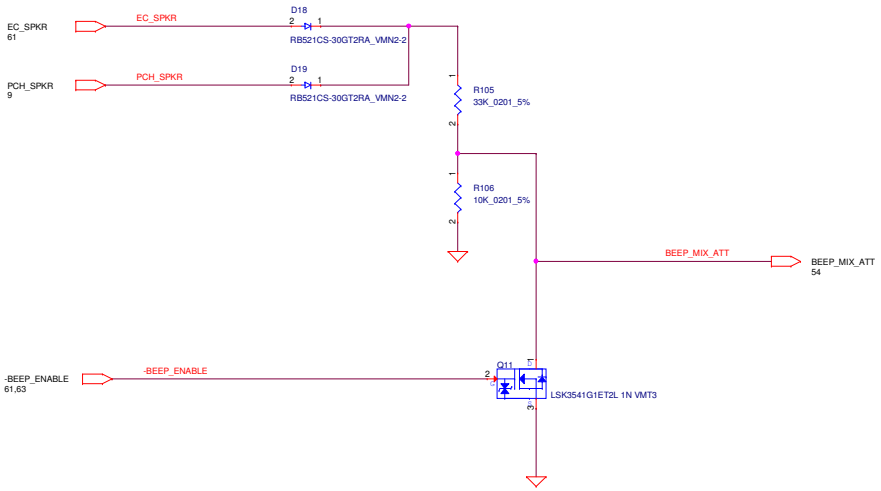

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Title: **AUDIO BEEP**

Size: Custom	Document Number: COBAIN SWG	Rev: 0.1
Date: Thursday, October 15, 2015	Sheet 59 of 97	

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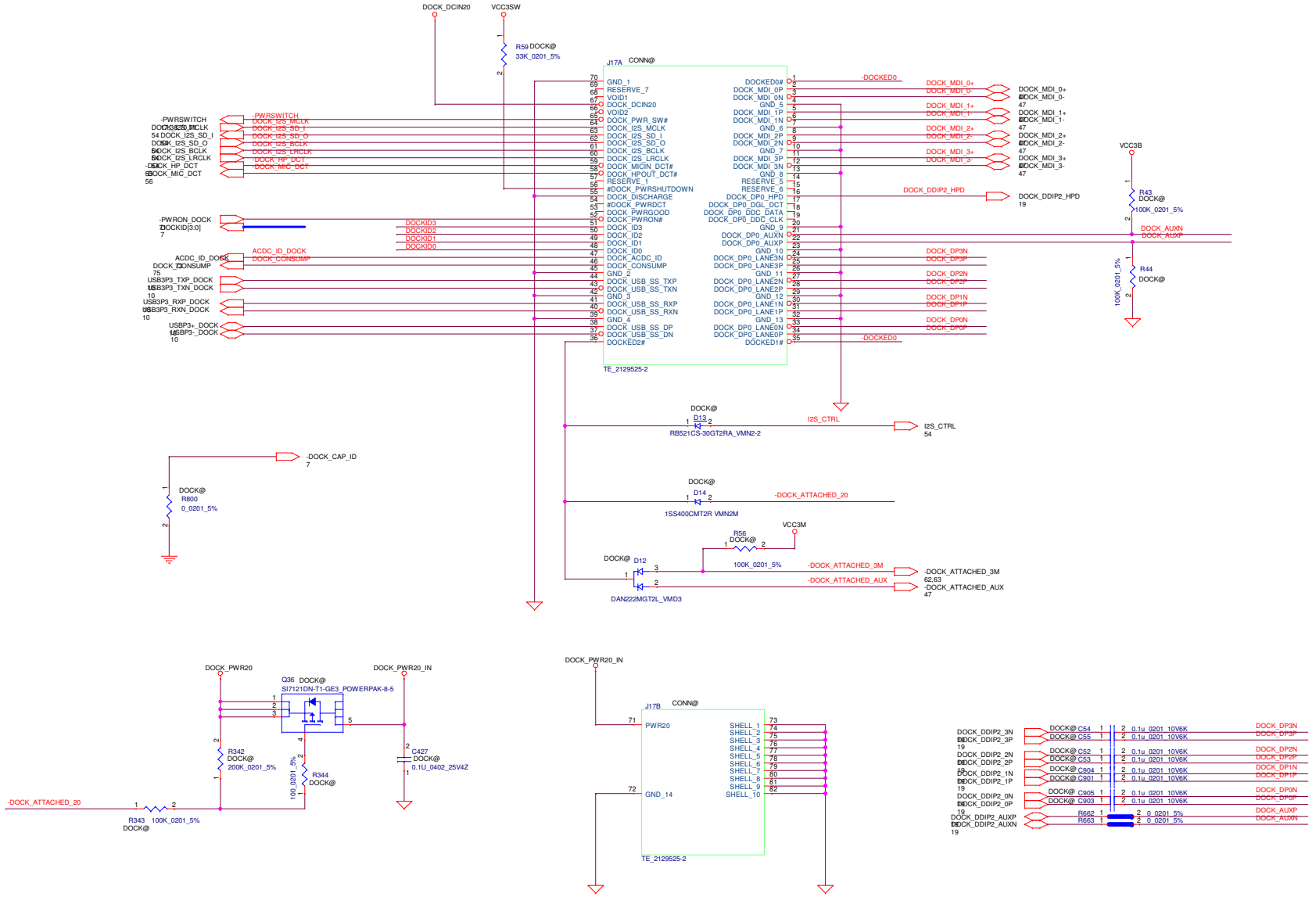

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Issued Date	2012/05/02	Deciphered Date	2012/5/02

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Title: DOCKING CONNECTOR

Size	Document Number	Rev
Custom	COBAIN3	0.1

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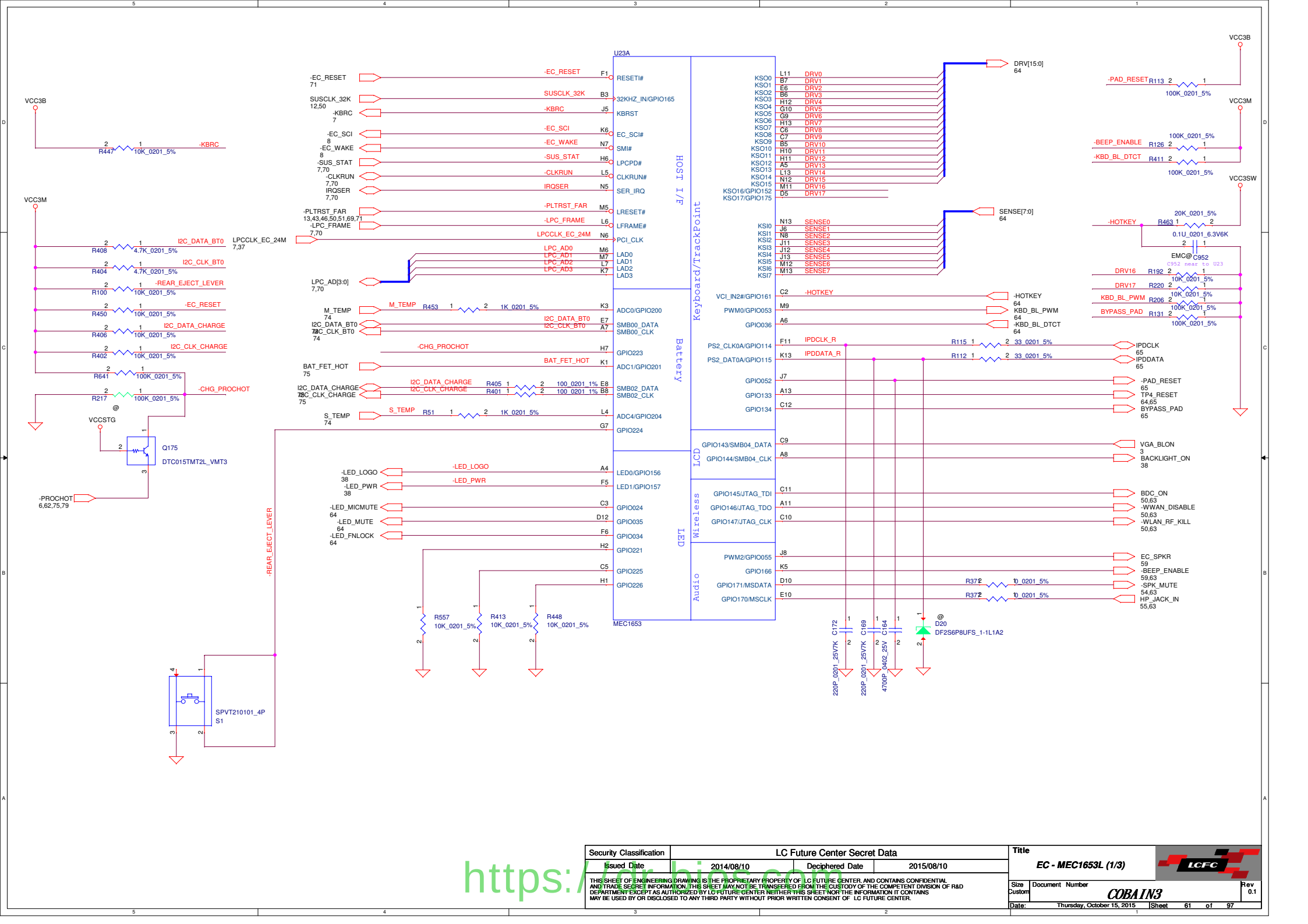

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Issued Date	2014/08/10	Deciphered Date	2015/08/10

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Title: EC - MEC1653L (1/3)

Size	Document Number	Rev
Custom	COBAIN3	0.1

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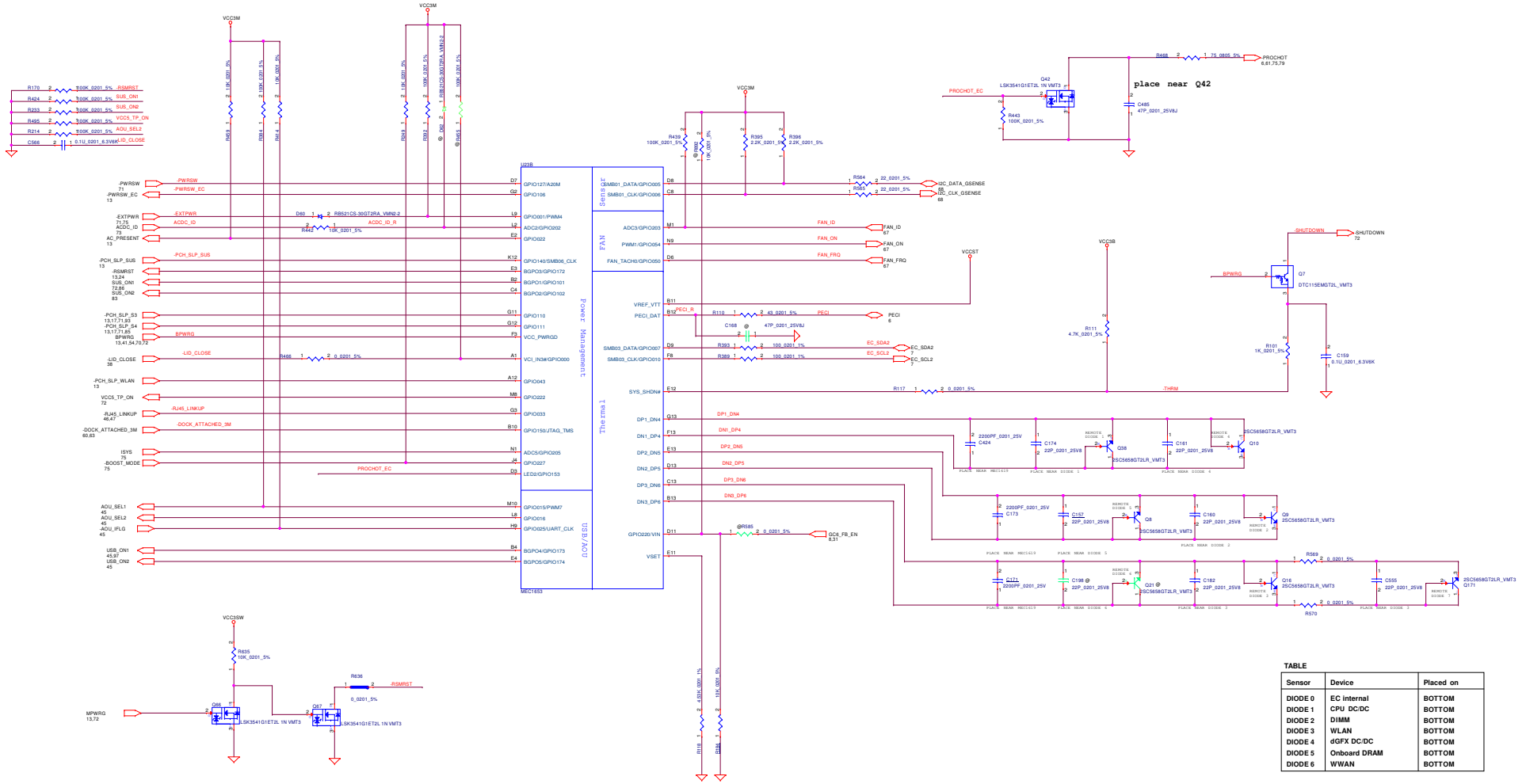
place near Q42
MEC1653
Sensor
FAN
Power Management
Thermal
TABLE
Sensor | Device | Placed on
DIODE 0 | EC internal | BOTTOM
DIODE 1 | CPU DC/DC | BOTTOM
DIODE 2 | DIMM | BOTTOM
DIODE 3 | WLAN | BOTTOM
DIODE 4 | dGFX DC/DC | BOTTOM
DIODE 5 | Onboard DRAM | BOTTOM
DIODE 6 | WWAN | BOTTOM

Security Classification	LC Future Center Secret Data		
Issued Date	2014/08/10	Deciphered Date	2015/08/10

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Title: EC - MEC1653L (2/3)

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Size: D | Document Number: CORAIN3 | Rev: 0.1

Date: Monday, October 05, 2015 | Sheet 62 of 97

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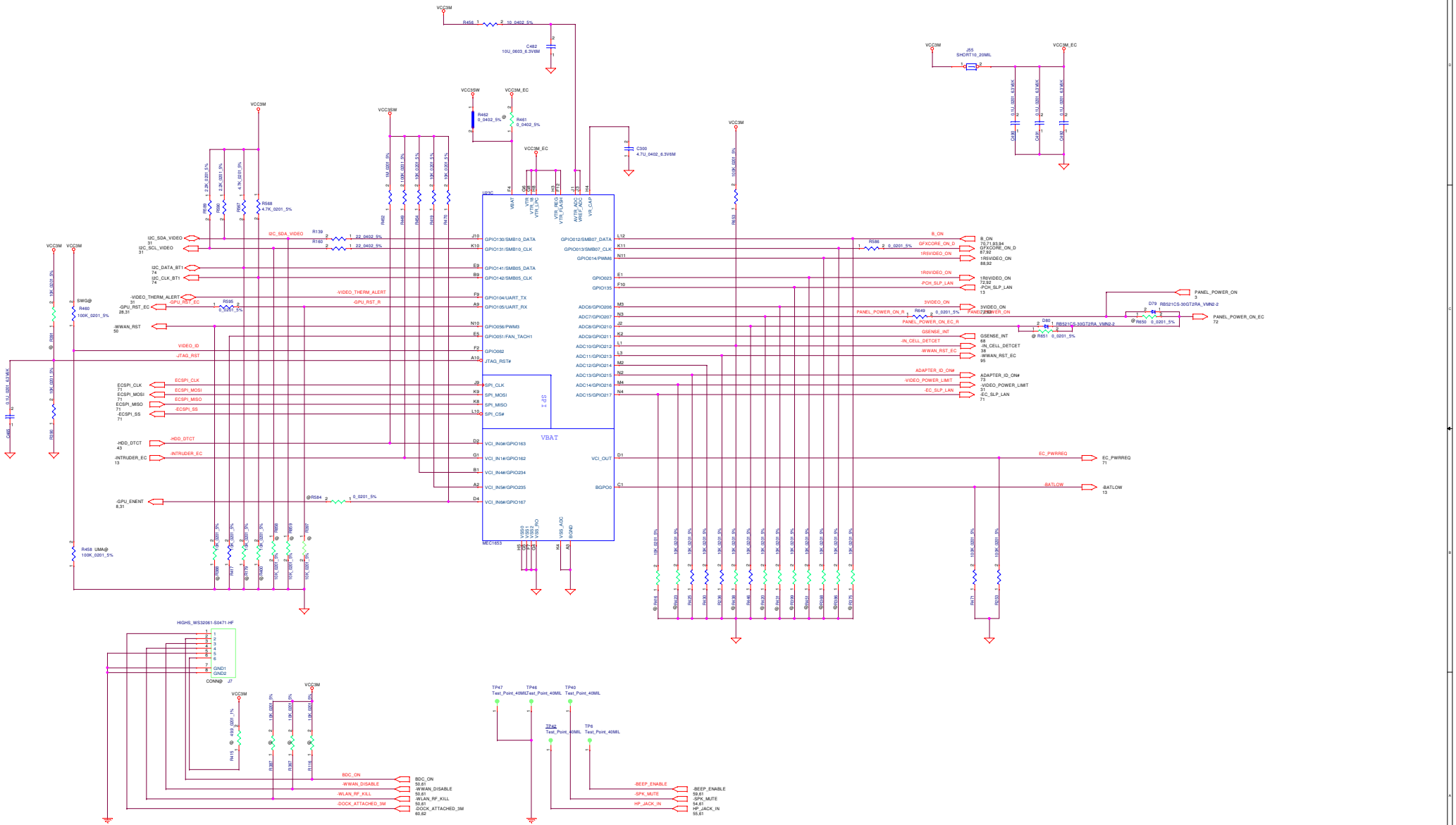

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Title: EC - MEC1653L (3/3)

Size	Document Number	Rev
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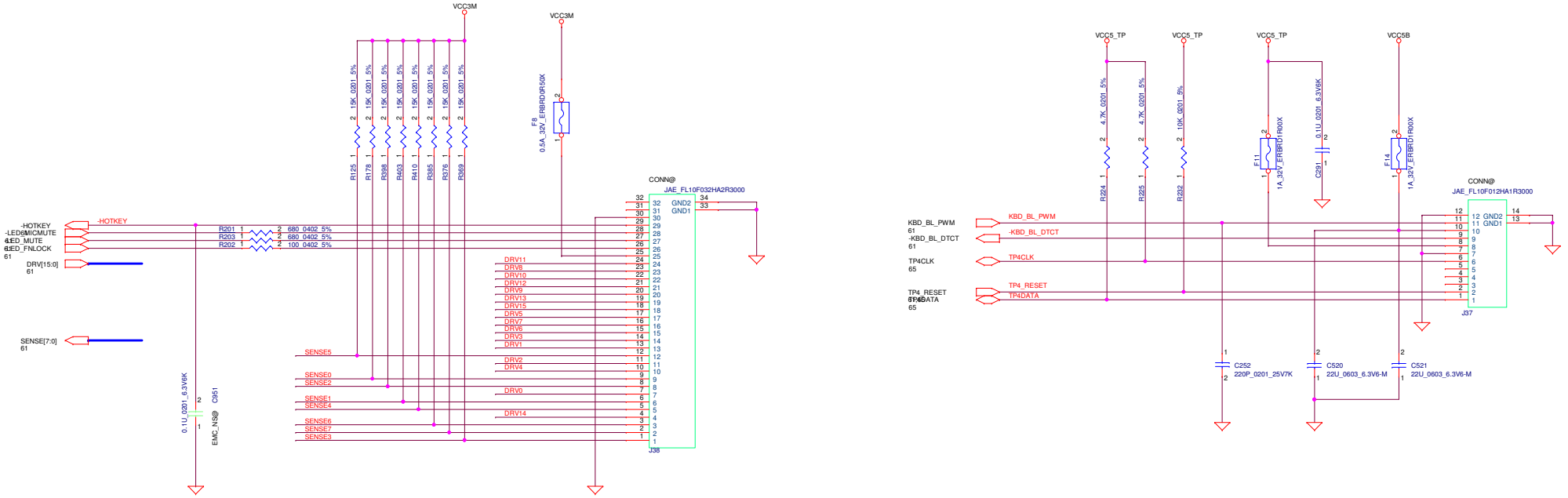

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/01	Deciphered Date	2012/12/01

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Title: KEYBOARD CONNECTOR

Size	Document Number	Rev
Custom	SWG COBAIN	0.1
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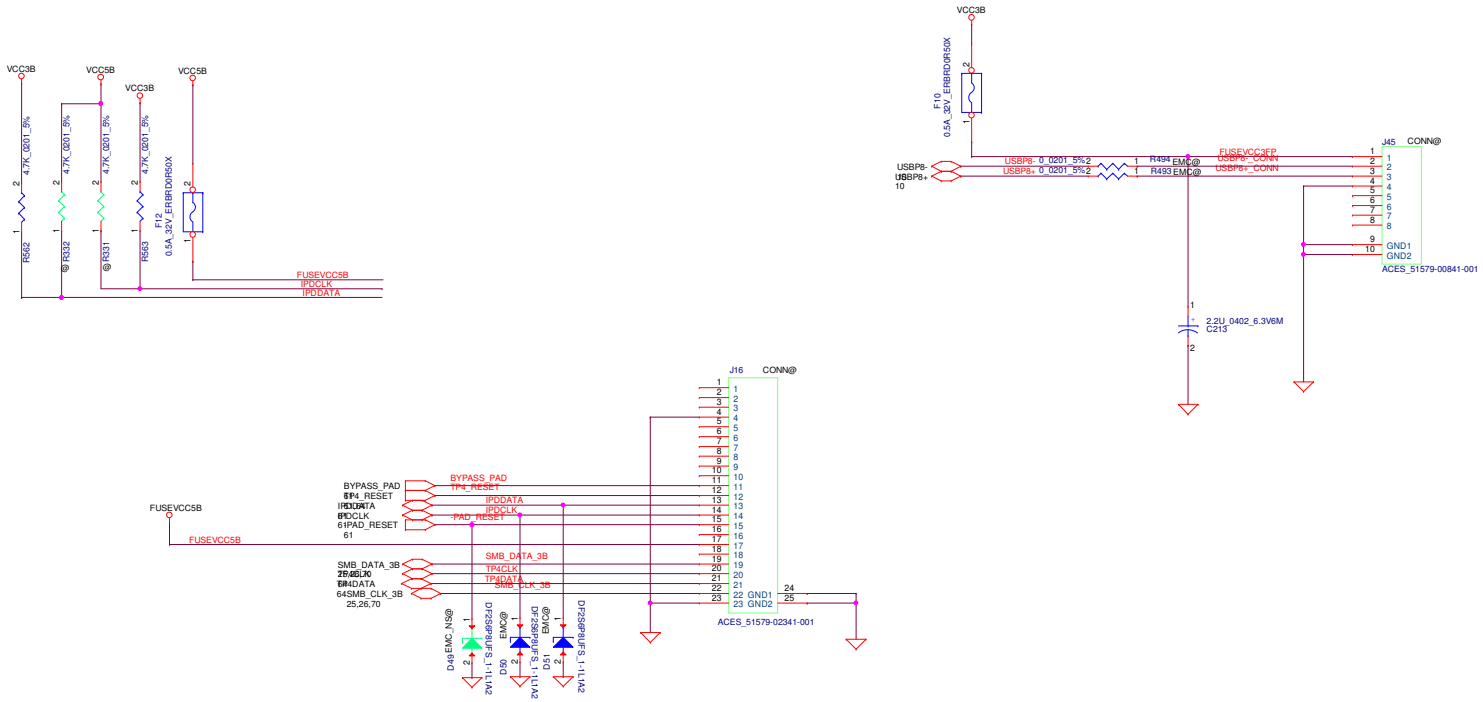

Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

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Title: TOUCH PAD CONNECTOR

Size	Document Number	Rev
Custom	COBAIN SWG	0.1

Date: Thursday, October 15, 2015 Sheet 65 of 97

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Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

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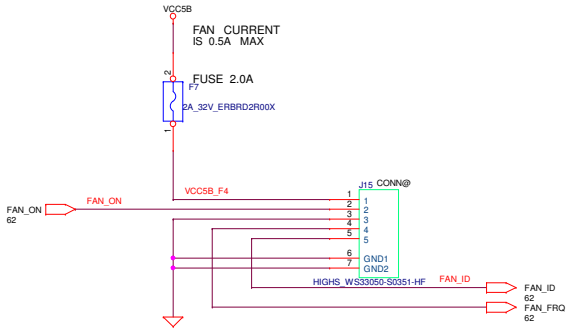
Title: BLANK

Size: Custom	Document Number: COBAIN SWG	Rev: 0.1
Date: Thursday, October 15, 2015	Sheet 66 of 97	

https://dr-bios.com



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Issued Date	2012/05/02	Deciphered Date	2012/5/02

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Title: FAN CONNECTOR

Size: Custom	Document Number: COBAIN SWG	Rev: 0.1
Date: Thursday, October 15, 2015	Sheet 67 of 97	

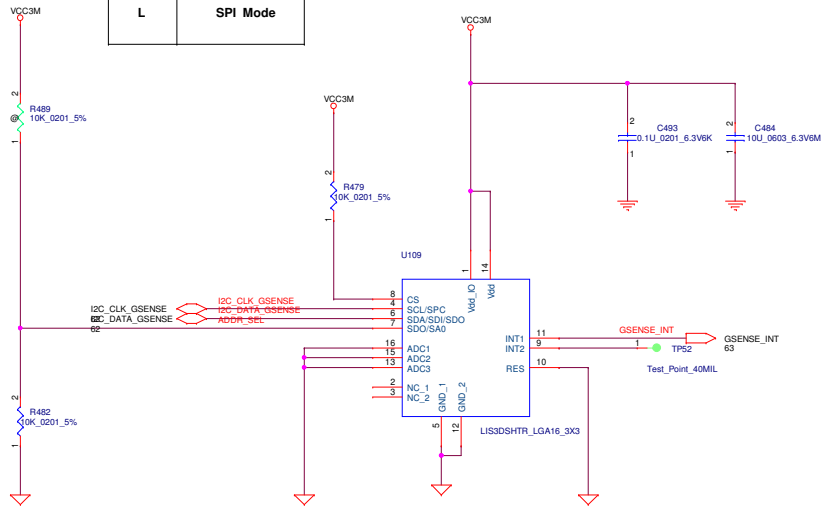
https://dr-bios.com

TABLE

P/N	ADDR_SEL	Address
LIS3DSH	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode



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Issued Date	2012/06/21	Deciphered Date	2012/06/21

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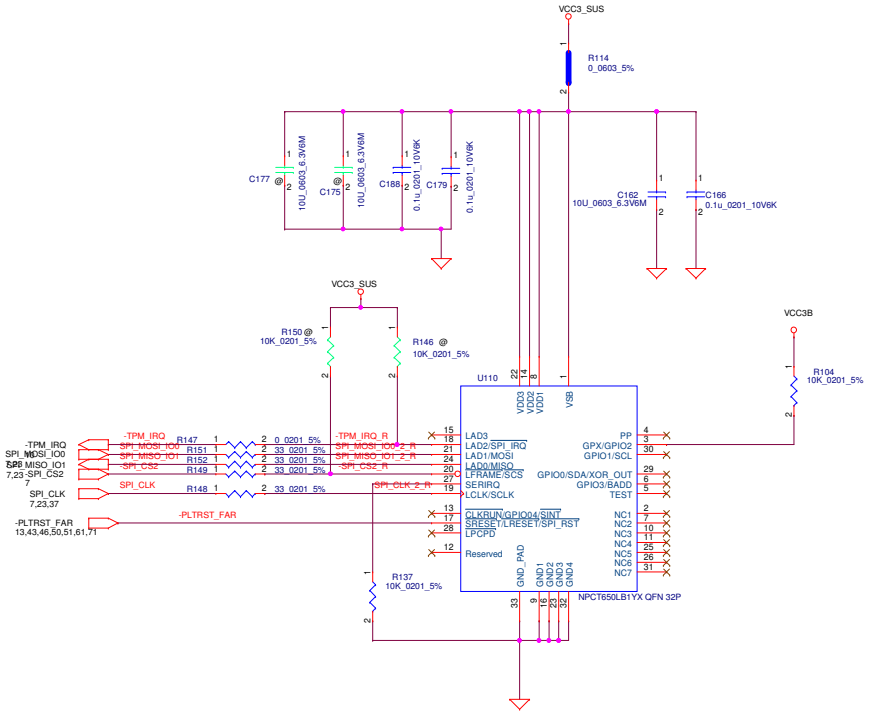
Title: G-SENSOR

Size	Document Number	Rev
Custom	COBAIN3	0.1

Date: Thursday, October 15, 2015 Sheet 68 of 97



Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

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Title: TPM

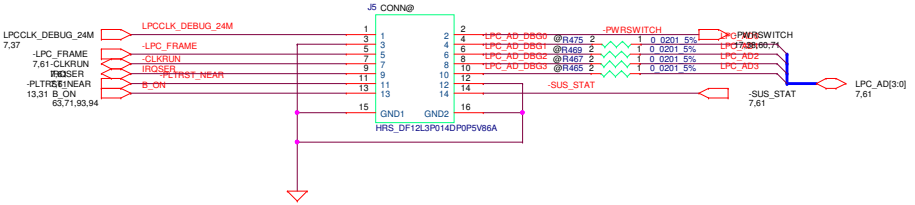
Size	Document Number	Rev
Custom	COBAIN3	0.1

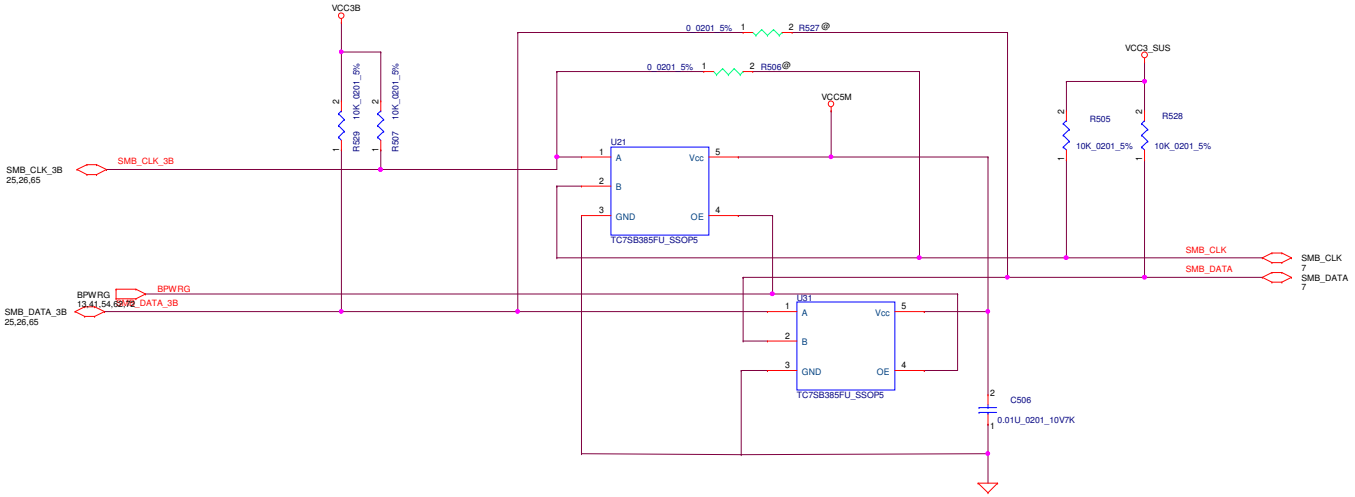
Date: Thursday, October 15, 2015 Sheet 69 of 97

https://dr-bios.com

LPC Debug port

	Planner Only	BOX
J5	ASM	NO_ASM
R9062	ASM	ASM





TABLE

EEPROM	U22	U23
U21	ASM	NO_ASM
U31	ASM	NO_ASM
C25	ASM	NO_ASM
R291	ASM	NO_ASM
Q84	ASM	NO_ASM
R8941	NO_ASM	ASM
R8940	NO_ASM	ASM
R30	ASM	NO_ASM
R45	ASM	NO_ASM

LOGIC

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

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Title	EEPROM/SMBUS SW		
Size	Document Number		Rev
Custom	COBAIN SWG		0.1
Date:	Thursday, October 15, 2015	Sheet	70 of 97

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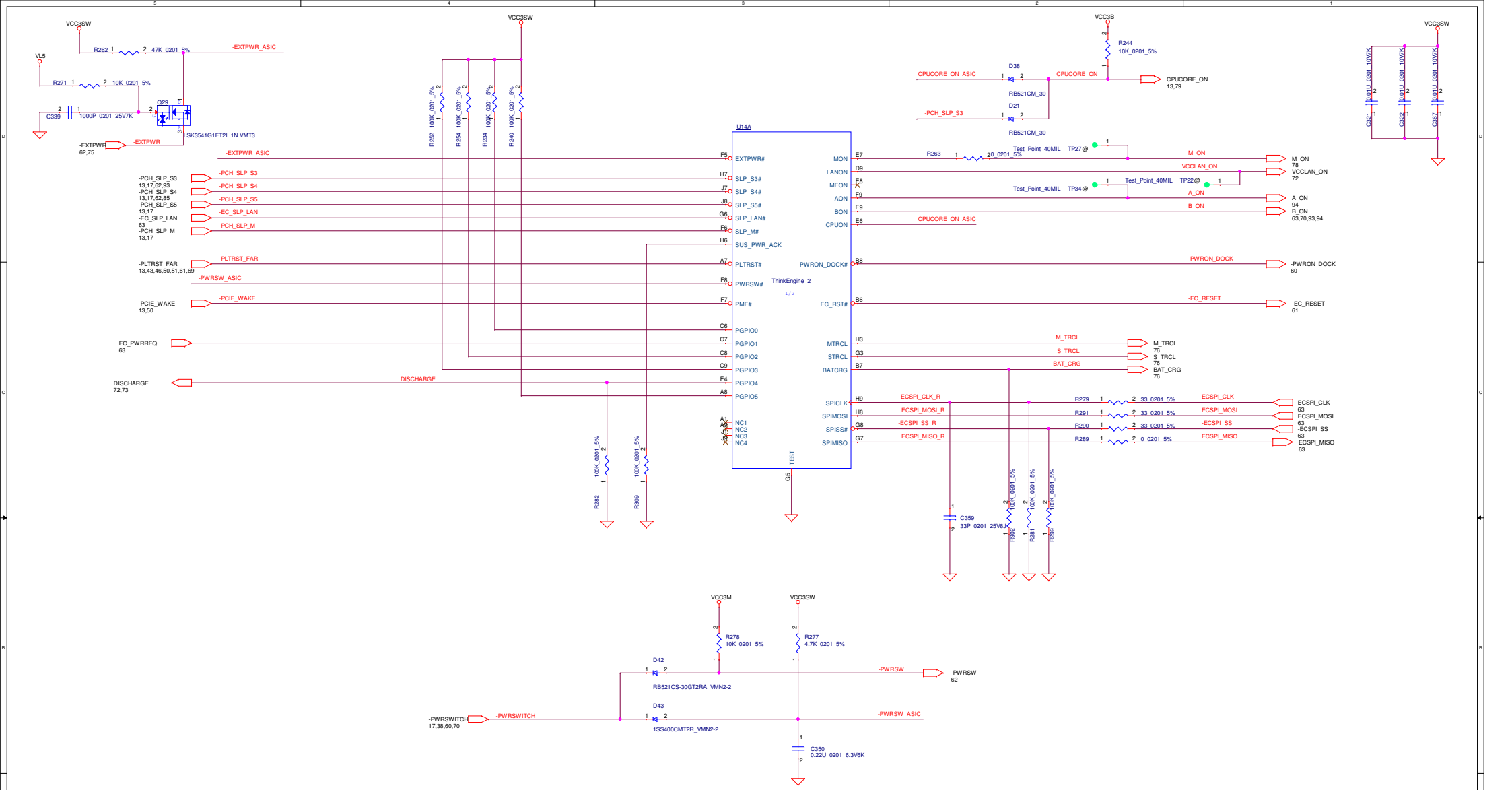

Security Classification	LC Future Center Secret Data		
Issued Date	2014/08/10	Deciphered Date	2015/08/10

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Title	THINK ENGINE(1/2)	
Size: Custom	Document Number: COBAIN3	Rev: 0.1
Date: Thursday, October 15, 2015	Sheet 71 of 97	

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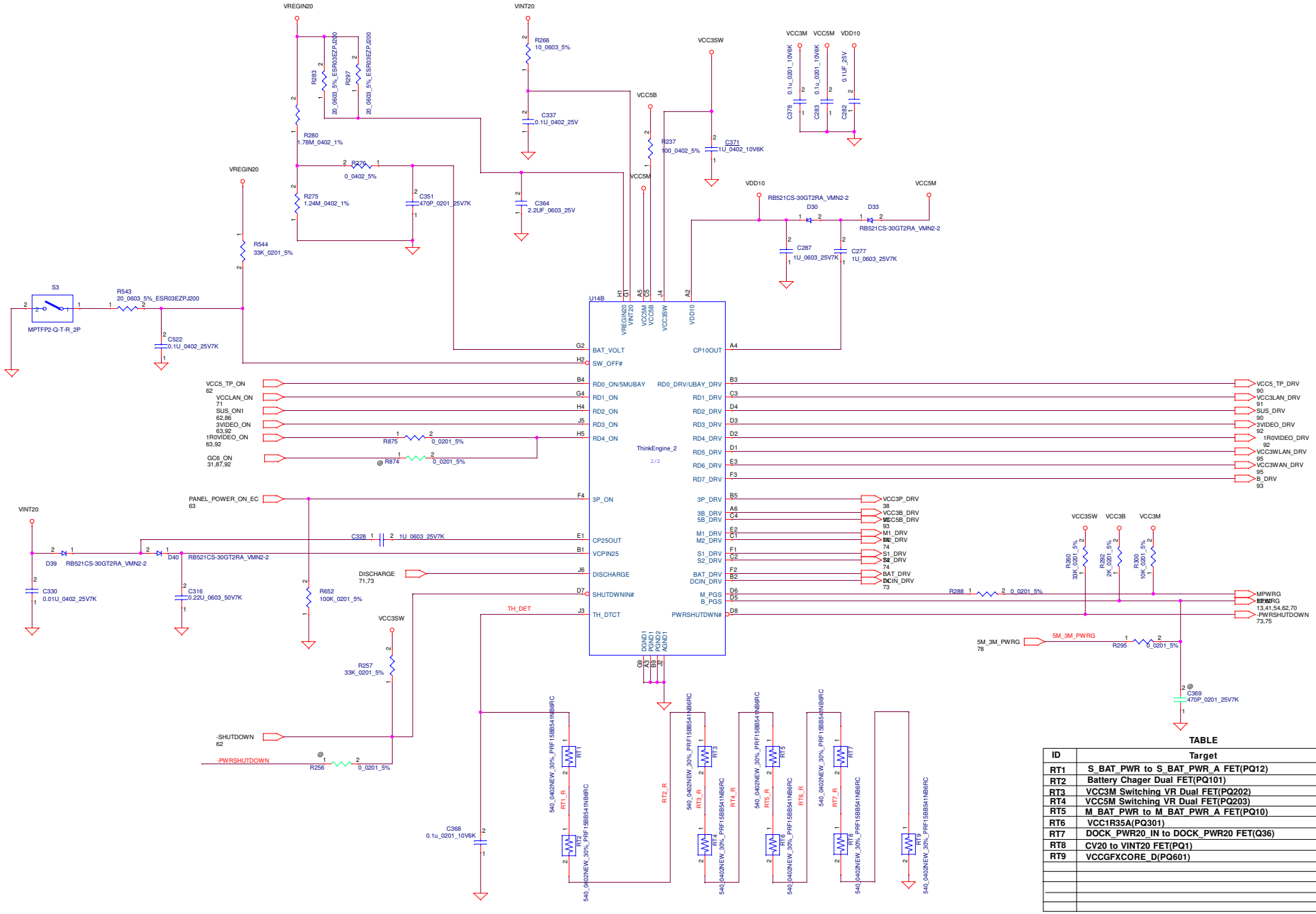

TABLE

ID	Target
RT1	S_BAT_PWR to S_BAT_PWR_A FET(PQ12)
RT2	Battery Chager Dual FET(PQ101)
RT3	VCC3M Switching VR Dual FET(PQ202)
RT4	VCC5M Switching VR Dual FET(PQ203)
RT5	M_BAT_PWR to M_BAT_PWR_A FET(PQ10)
RT6	VCC1R35A(PQ301)
RT7	DOCK_PWR20_IN to DOCK_PWR20 FET(Q36)
RT8	CV20 to VINT20 FET(PQ1)
RT9	VCCGFXCORE_D(PQ601)

Security Classification	LC Future Center Secret Data		
Issued Date	2014/08/10	Deciphered Date	2015/08/10

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Title: THINK ENGINE(2/2)

Size: Custom | Document Number: COBAIN3 | Rev: 0.1

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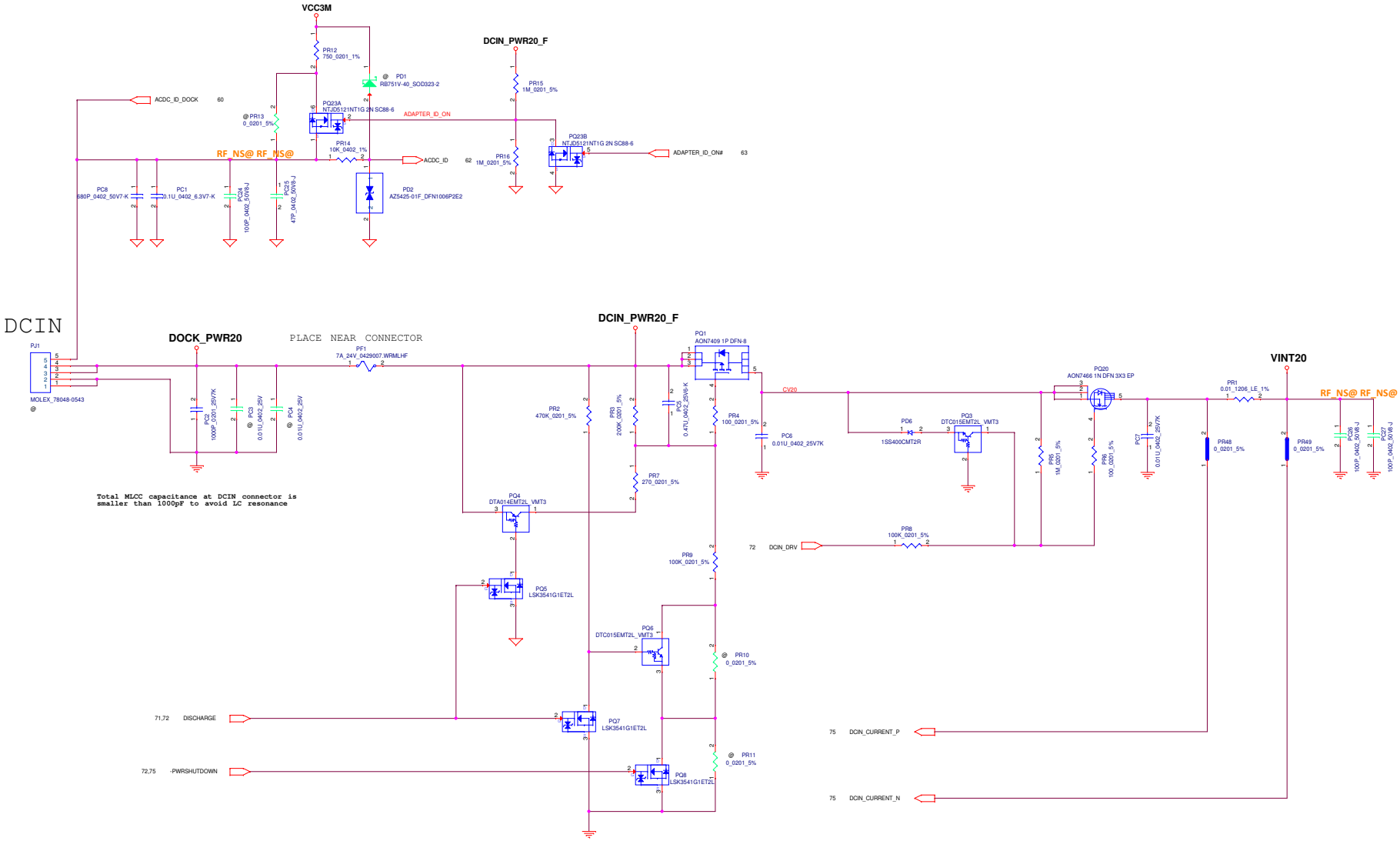

TABLE

PEAK SHIFT	YES	NO
RR10	NO-ASM	ASM
PR2	ASM	NO-ASM
PQ7	ASM	NO-ASM
PQ6	ASM	NO-ASM

LOGIC

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Security Classification	LC Future Center Secret Data	Title	DC-IN
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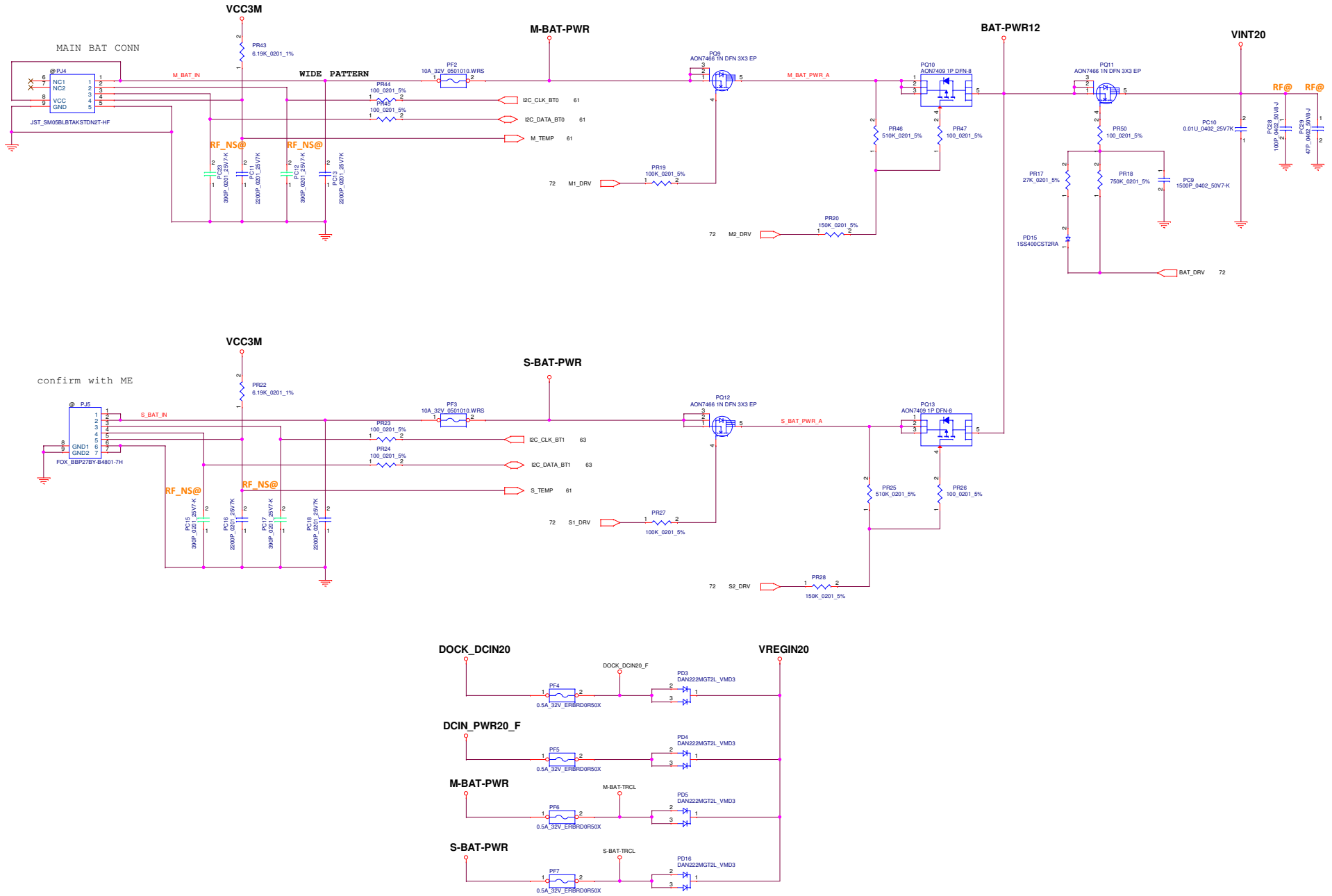
		Date: Thursday, October 15, 2015	Sheet 73 of 95



Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	

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Title: **BATTERY INPUT**

Size	Document Number	Rev
Custom	Cobain3 Intel	0.1
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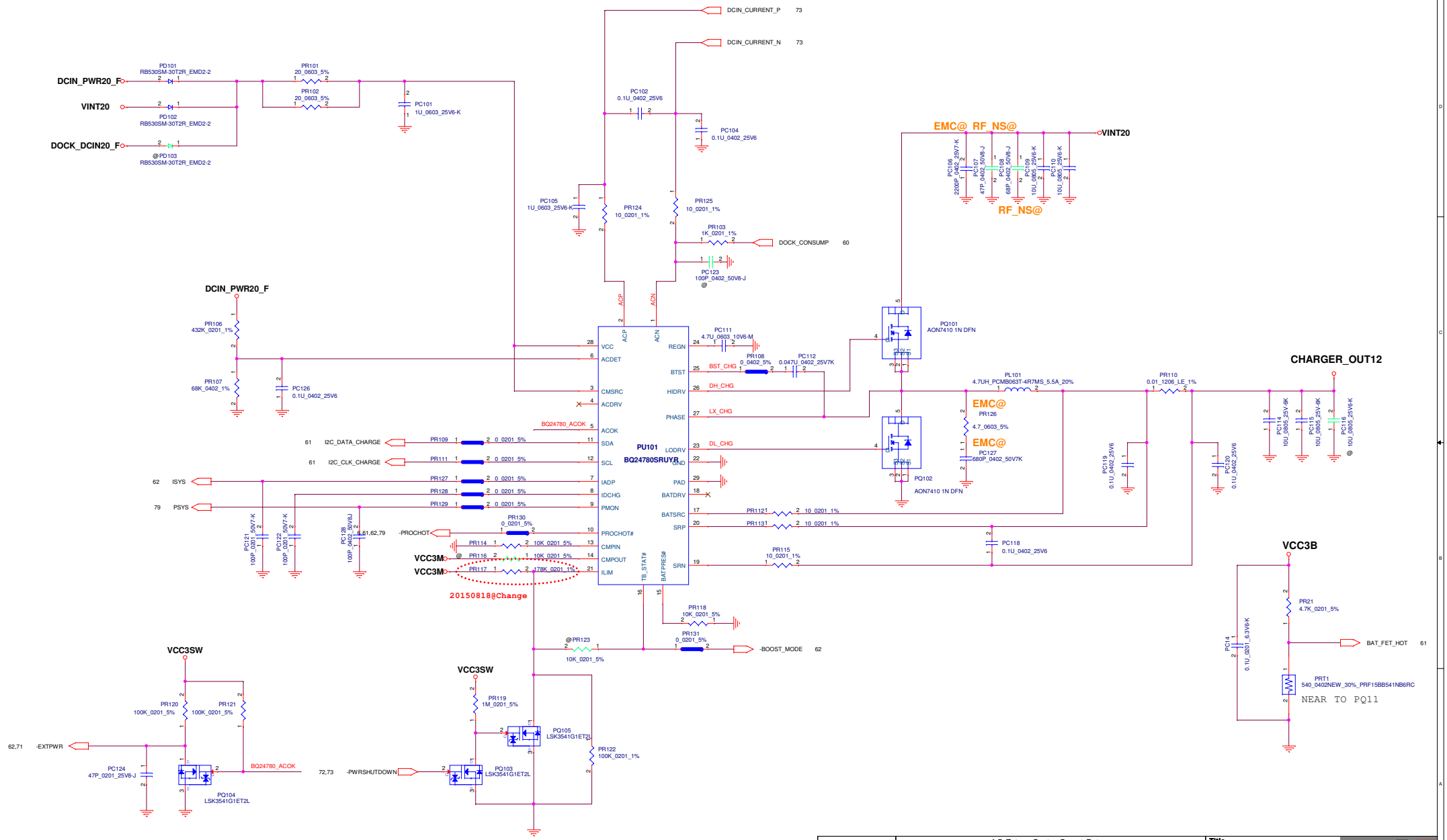
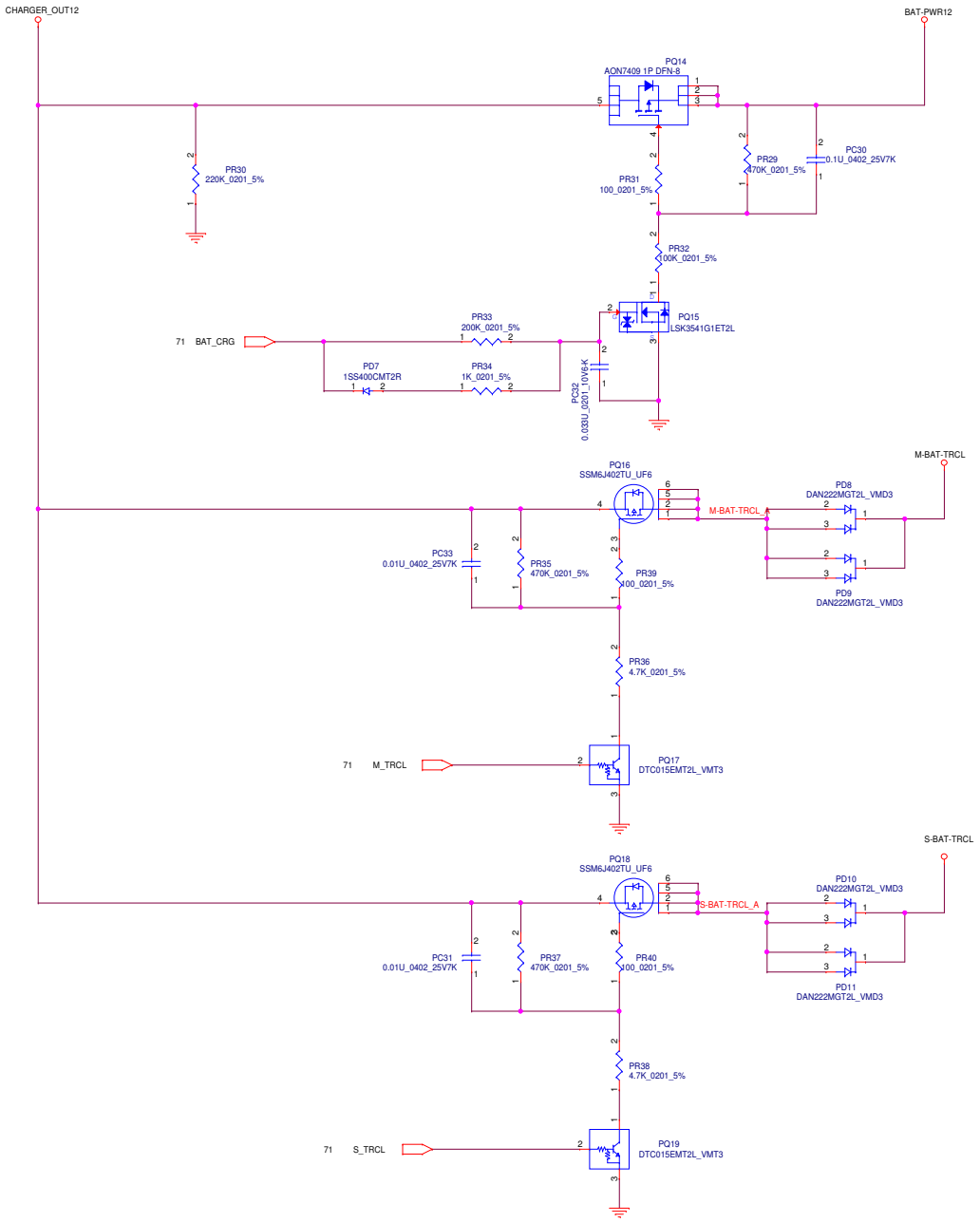


https://dr-bios.com



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Security Classification	LC Future Center Secret Data	Title	CHARGER SELECTOR
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Size	Document Number	Rev
C	Cobain3 Intel	0.1

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Title: Blank		
Size: Custom	Document Number: Cobain3 Intel	Rev: 0.24
Date: Thursday, October 15, 2015	Sheet 77 of 95	

All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

VCC5M
TDC= 8A
OCP =12A

VCC3M
TDC= 8A
OCP =12A

VINT20
5V_VIN
EMC@ RF@ RF@ EMC@
@PJ201 JUMP_43X79
PC203 10U_0805_25V6K
PC204 10U_0805_25V6K
PC205 0.1U_0402_25V6-K
PC219 47P_0402_50V8-J
PC226 100P_0402_50V8-J
PC113 2200P_0402_25V7-K

VINT20
VL5
71 M_ON
PR221 0_0201_5%
@PC211 0.01U_0402_25V
PC212 4.7U_0402_6.3V
PC213 4.7U_0402_6.3V

PQ201 AON7410 1N DFN
PQ203 AON7534 1N DFN

VCC5MP
EMC@ EMC@
PL201 2.2UH_PCMB063T-2R2MS_8A_20%
PC210 0.1U_0402_25V7-K
PC125 2200P_0402_25V7-K
PC222 220U_B2_6.3VM_R35M
PC223 220U_B2_6.3VM_R35M
PC224 0.01U_0201_6.3V7-K
PR210 150K_0201_1%
PR212 4.7_0603_5%
EMC_NS@
PC216 680P_0402_50V7K
EMC_NS@
PR215 0_0201_5%
PR220 100K_0201_1%

PU201
TPS51285BRUKR_WQFN20_3X3
EN1 DRVH1 VBST1 SW1 DRVL1 VO1 VFB1
VIN VREG5 VREG3 CS1 CS2 GND PGOOD VCLK
EN2 DRVH2 VBST2 SW2 DRVL2 VFB2

VCC5M_DH
VCC5M_BST
VCC5M_LX
VCC5M_DL
VCC5M_FB1
PR209 0_0402_5%
PC214 0.1U_0402_25V7-K
PC225 0.1U_0201_6.3V6K
PR216 200_0201_1%
PR217 11.8K_0201_1%
PR218 13.3K_0201_1%

VCC3M_DH
VCC3M_BST
VCC3M_LX
VCC3M_DL
VCC3M_VFB2
PR208 0_0402_5%
PC215 0.1U_0402_25V7-K
PR222 0_0201_5%
5M_3M_PWRG 72

PQ202 AON7410 1N DFN
PQ204 AON7534 1N DFN
PC117 2200P_0402_25V7-K
PC221 100P_0402_50V8-J
PC207 47P_0402_50V8-J
PC206 0.1U_0402_25V6-K
PC208 10U_0805_25V6K
PC209 10U_0805_25V6K
@PJ202 JUMP_43X79
3V_VIN
VINT20

PR213 4.7_0603_5%
EMC_NS@
PC217 680P_0402_50V7K
EMC_NS@
PR211 130K_0201_1%
PC218 0.01U_0201_6.3V7-K
PR214 0_0201_5%
PR219 200K_0201_1%

VCC3MP
PL202 2.2UH_PCMB063T-2R2MS_8A_20%
EMC@ EMC@
PC220 220U_B2_6.3VM_R35M
PC227 0.1U_0402_25V7-K
PC129 2200P_0402_25V7-K

VCC3MP
@PJ203 JUMP_43X118
VCC3M

VCC5MP
@PJ204 JUMP_43X118
VCC5M

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Title: DC/DC VCC5M/VCC3M(TPS51285B)

Size	Document Number	Rev
Custom	Cobain3 Intel	0.1

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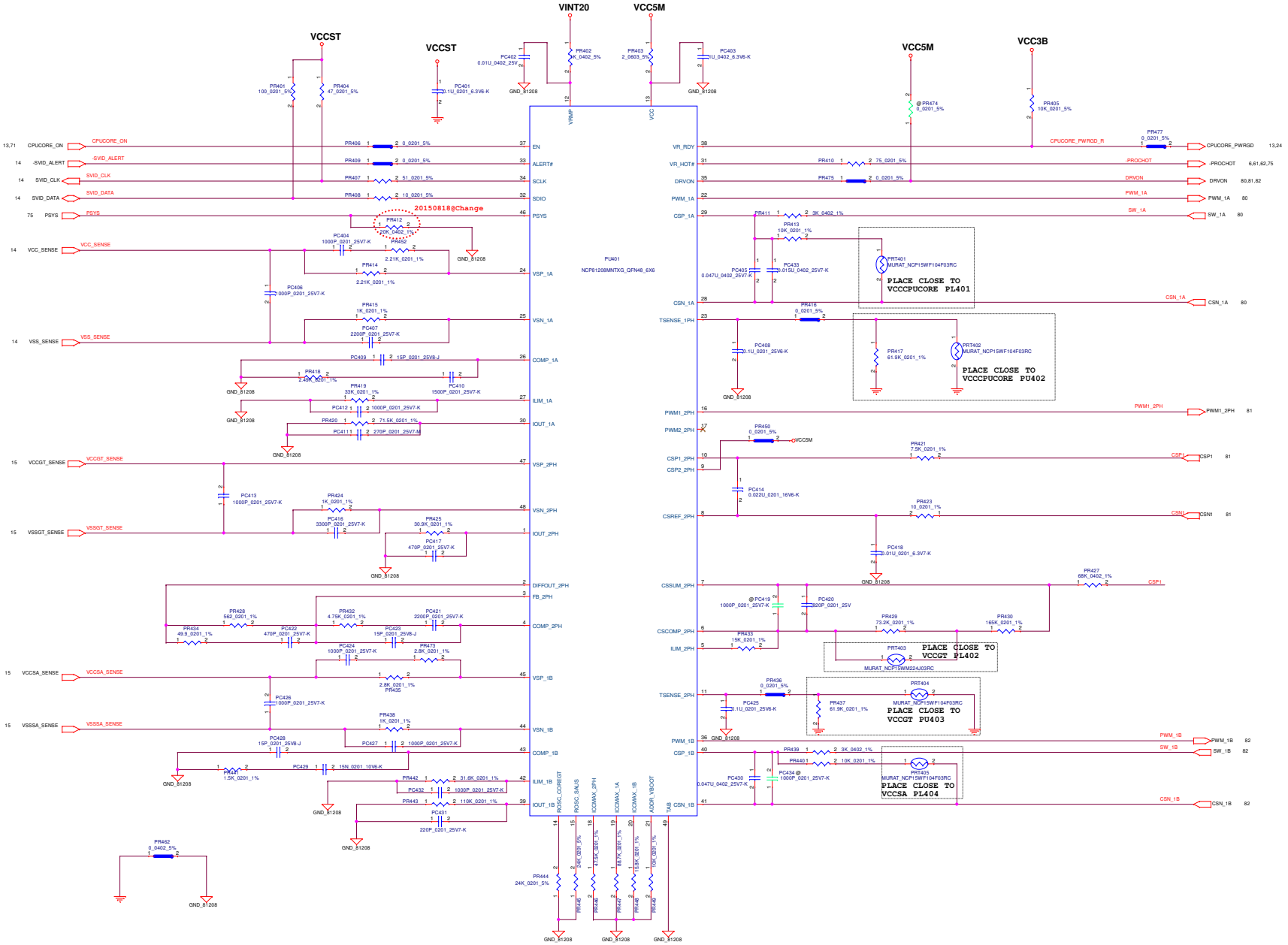

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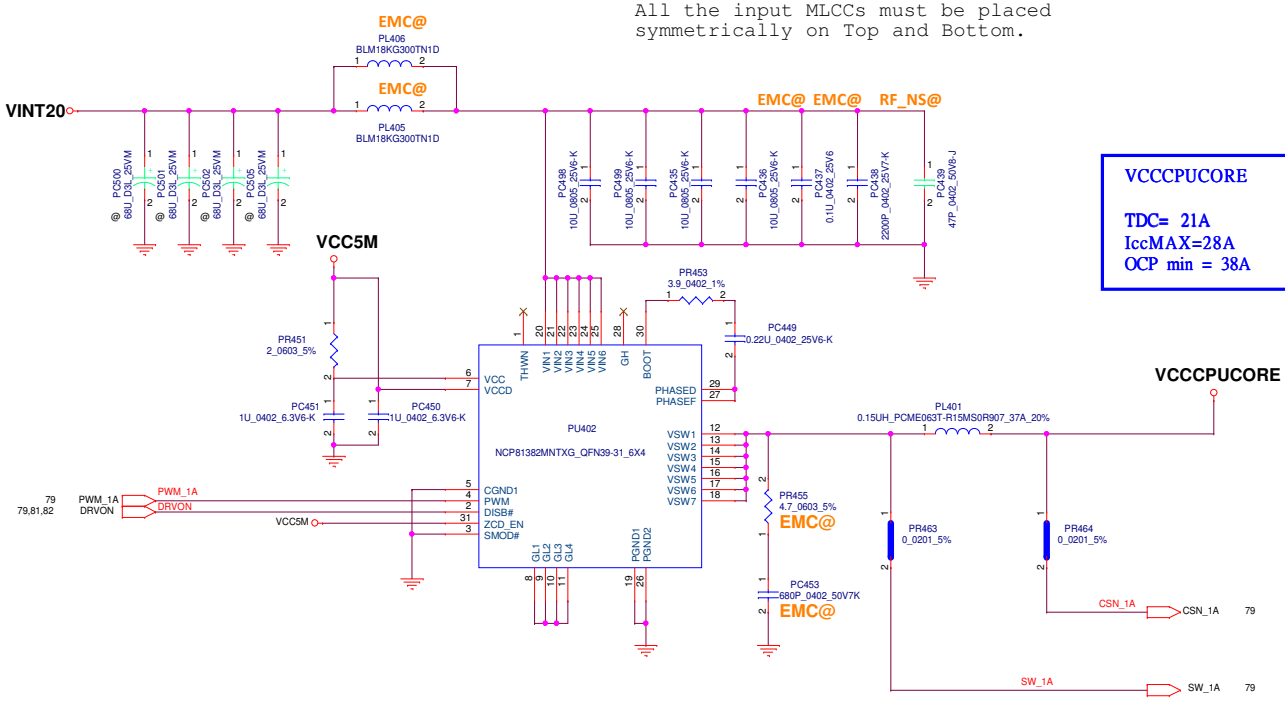
Title: DC/DC IMVP8(NCP81208)

LCFC

Size	Document Number	Rev
Custom	Cobain3 Intel	0.1

Date: Thursday, October 15, 2015 Sheet 79 of 95

All the input MLCCs must be placed
symmetrically on Top and Bottom.

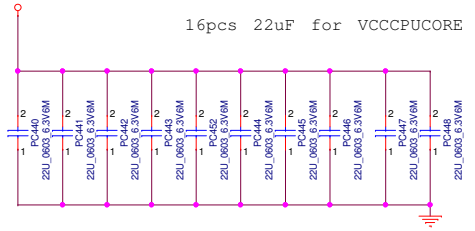


VCCCPUCORE

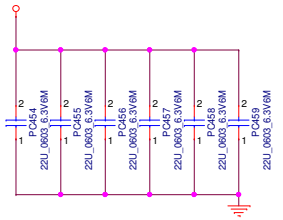
TDC= 21A
IccMAX=28A
OCP min = 38A

VCCCPUCORE

16pcs 22uF for VCCCPUCORE



VCCCPUCORE



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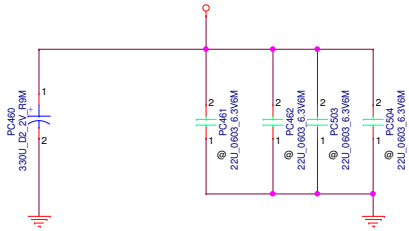

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Title: DC/DC CPUCORE(NCP81382)

Size	Document Number	Rev
Custom	Cobain3 Intel	0.1

Date: Thursday, October 15, 2015 Sheet 80 of 95

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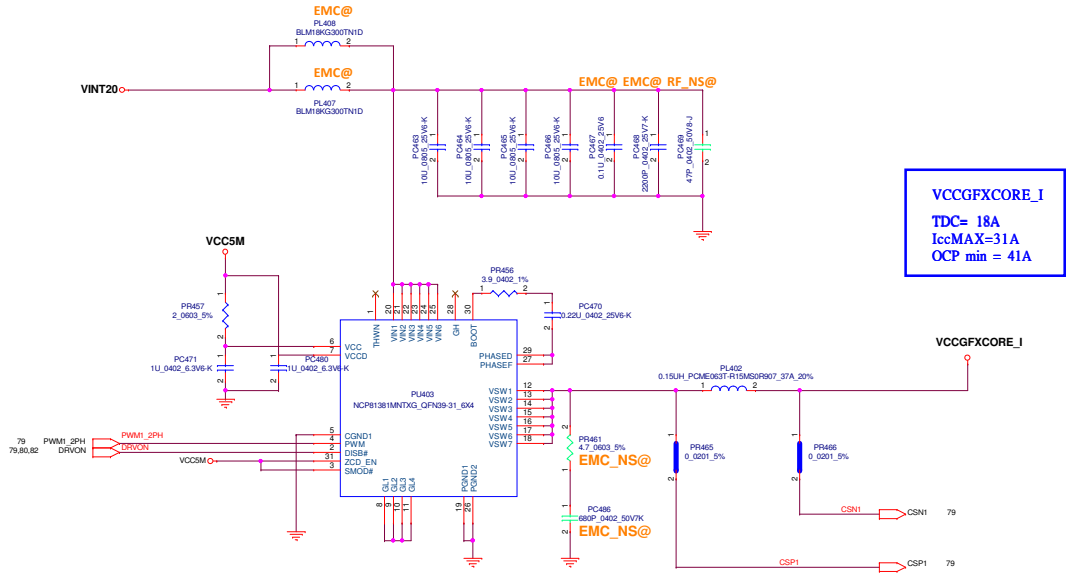
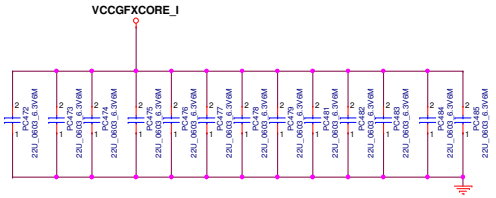
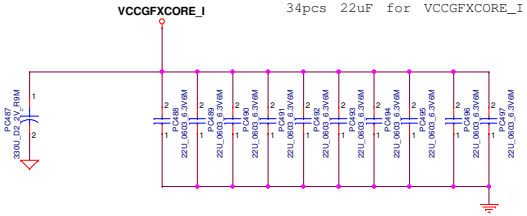
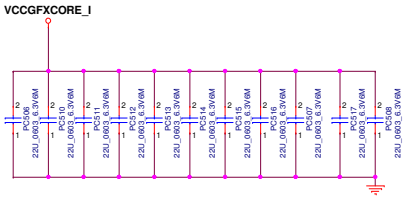


VCCGFXCORE_I

TDC= 18A
IccMAX=31A
OCP min = 41A







Security Classification	LC Future Center Secret Data		Title: DC/DC VCCGFXCORE_I(NCP81382)
Issued Date		Deciphered Date	

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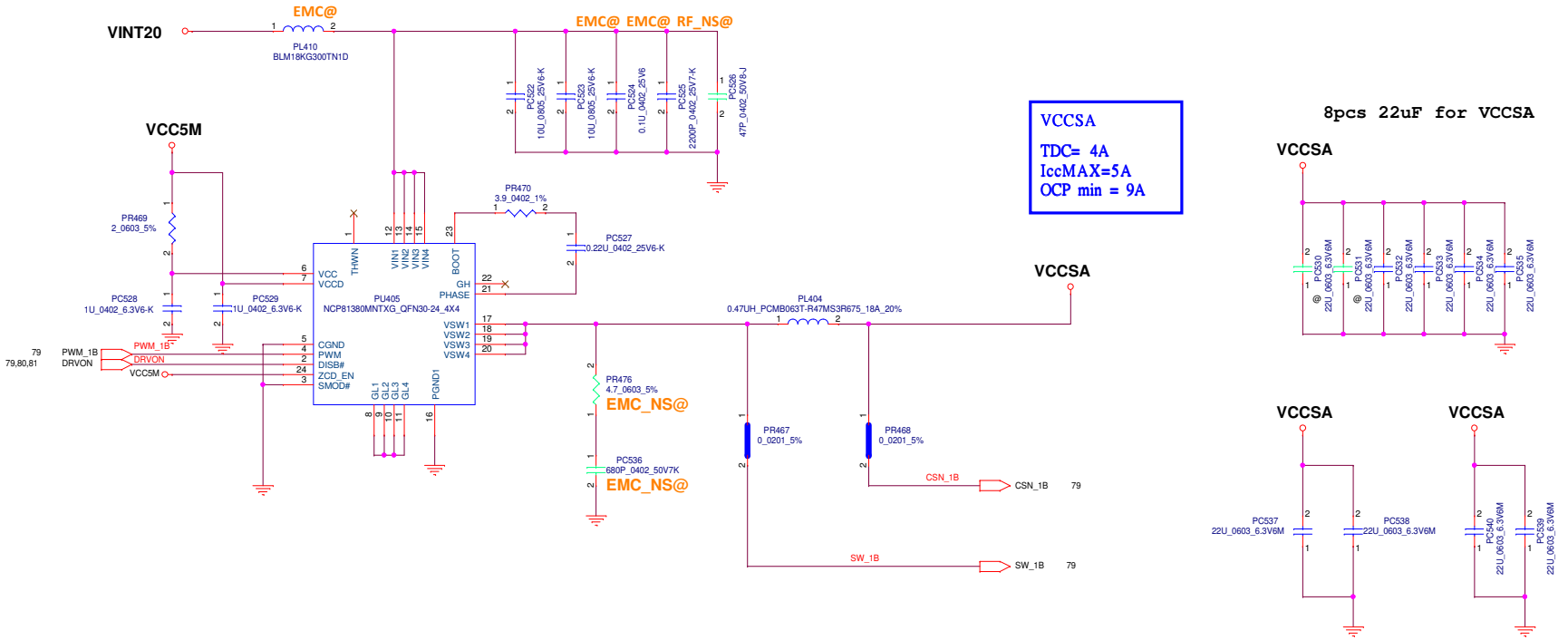
All the input MLCCs must be placed
symmetrically on Top and Bottom.



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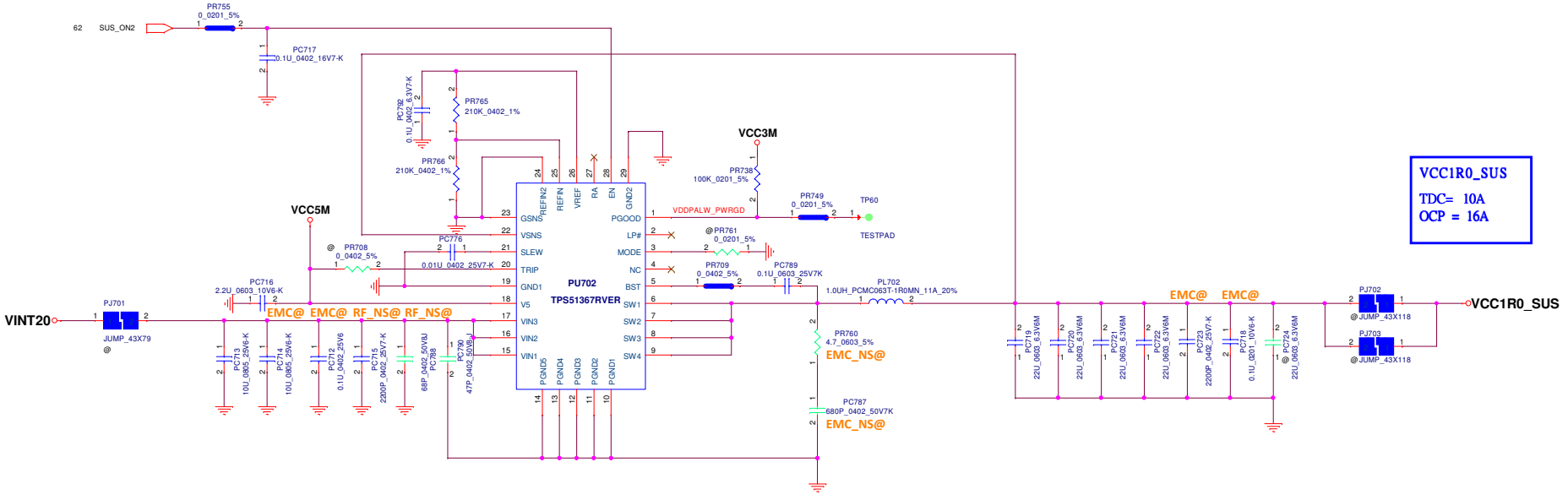

Mode	Frequency
GND	400KHz
Float	800KHz

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Title: DC/DC VCC1R0_SUS(TPS51367)

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Size: Custom	Document Number: *Cobain3 Intel*	Rev: 0.1
Date: Thursday, October 15, 2015	Sheet 84 of 95	

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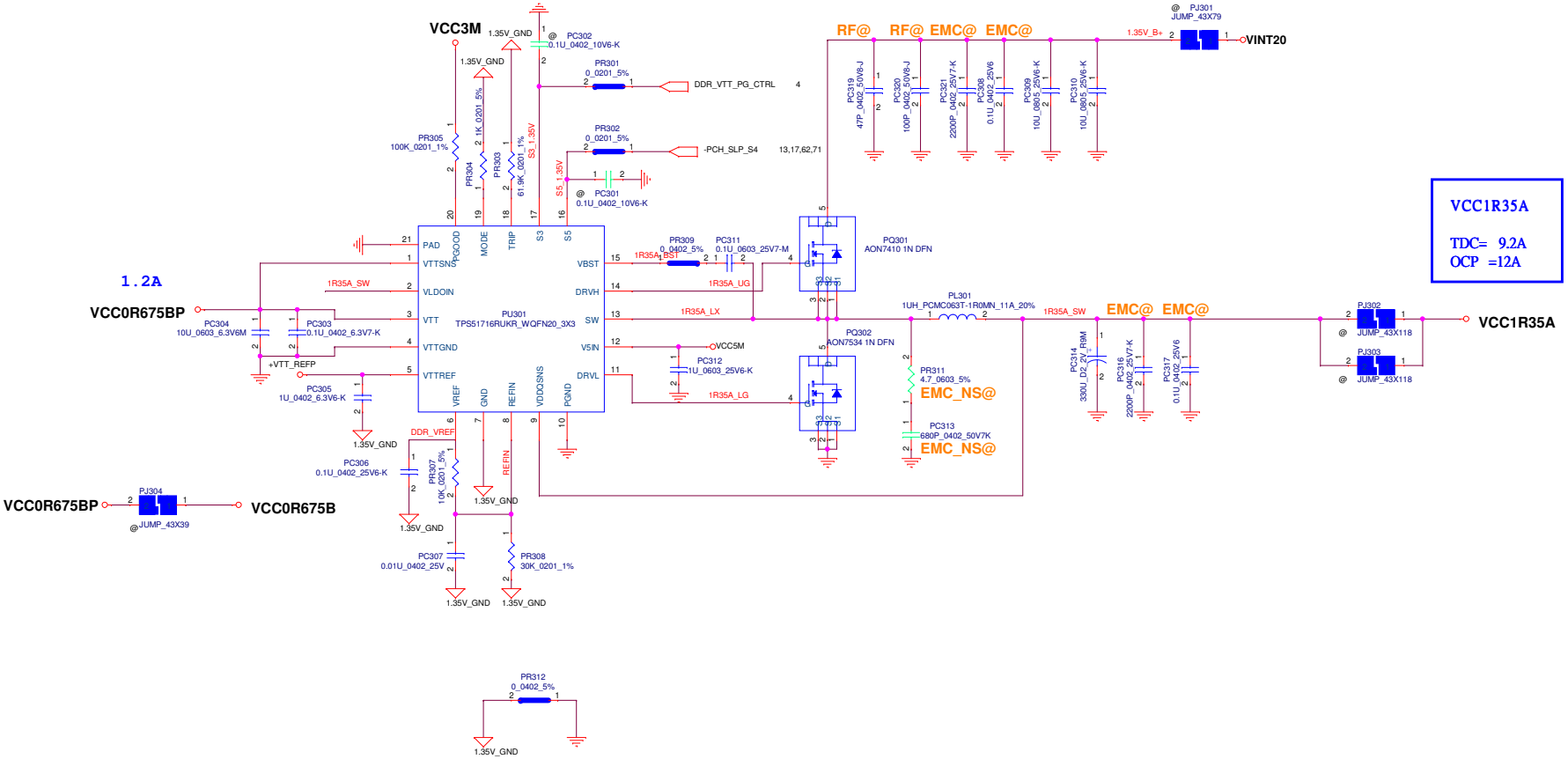

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Title	DC/DC VCC1R35A(TPS51716)		
Size: Custom	Document Number: Cobain3 Inel		Rev: 0.1
Date: Thursday, October 15, 2015	Sheet 85 of 95		

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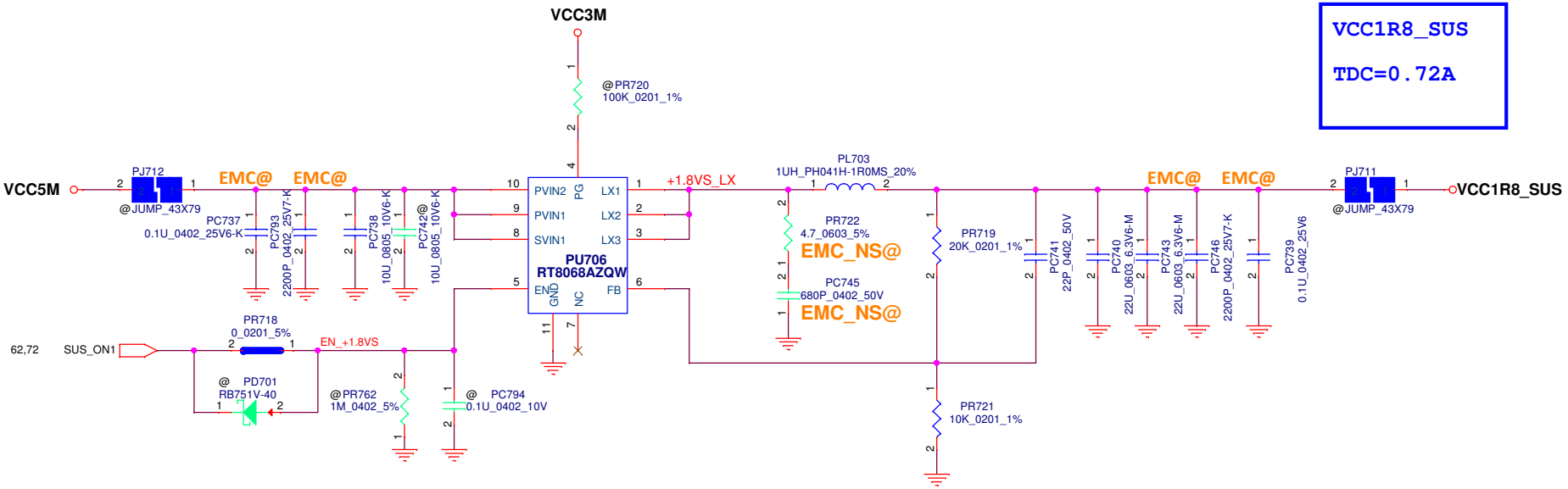

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Issued Date	2013/08/01	Deciphered Date	2014/08/01

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Title: *DC/DC VCC1R8_SUS(RT8068A)*

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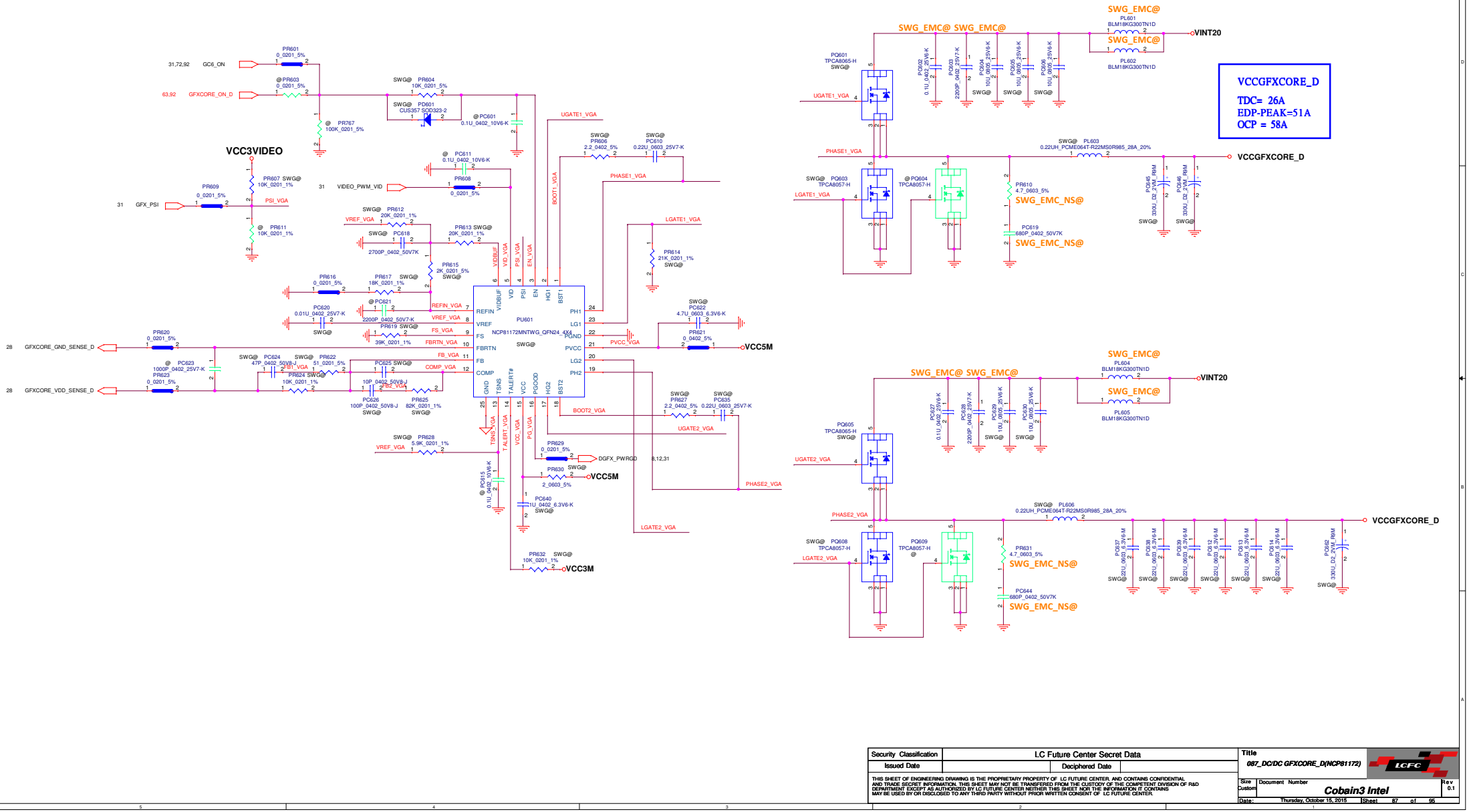

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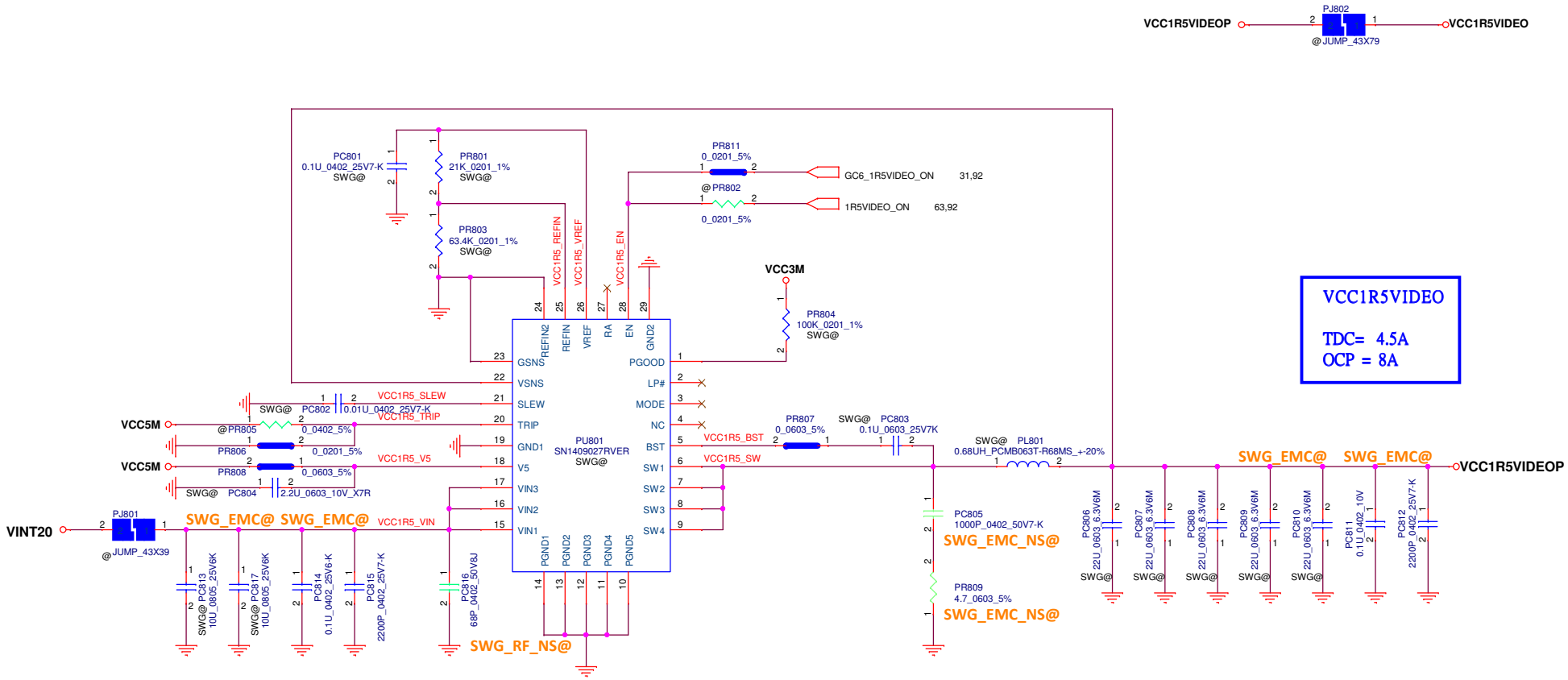

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Title	DC/DC VCC1R5VIDEO(SN1409027)	
Size: Custom	Document Number: Cobain3 Intel	Rev: 0.1
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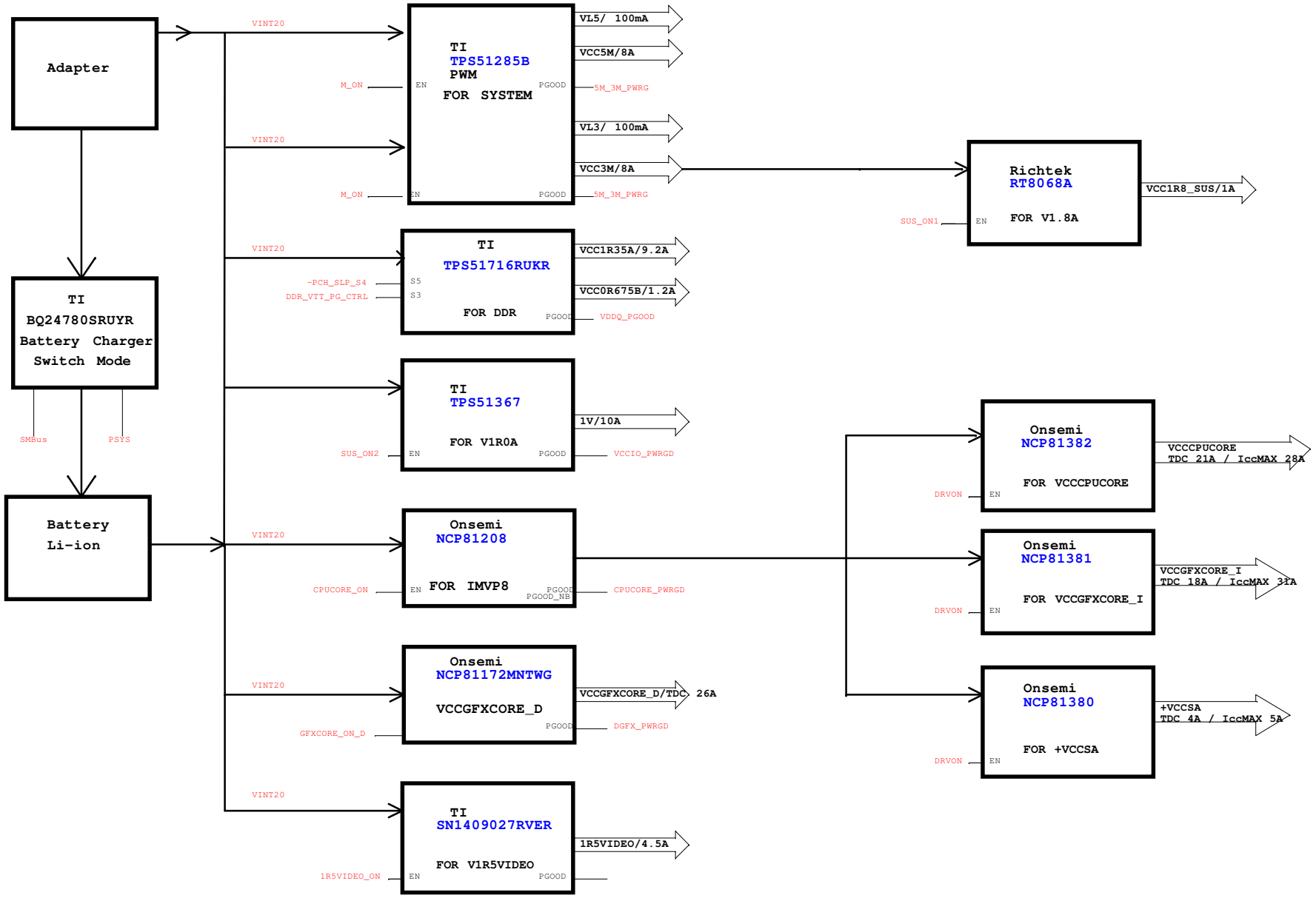

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Size: Custom	Document Number: WV3		Rev: 0.1
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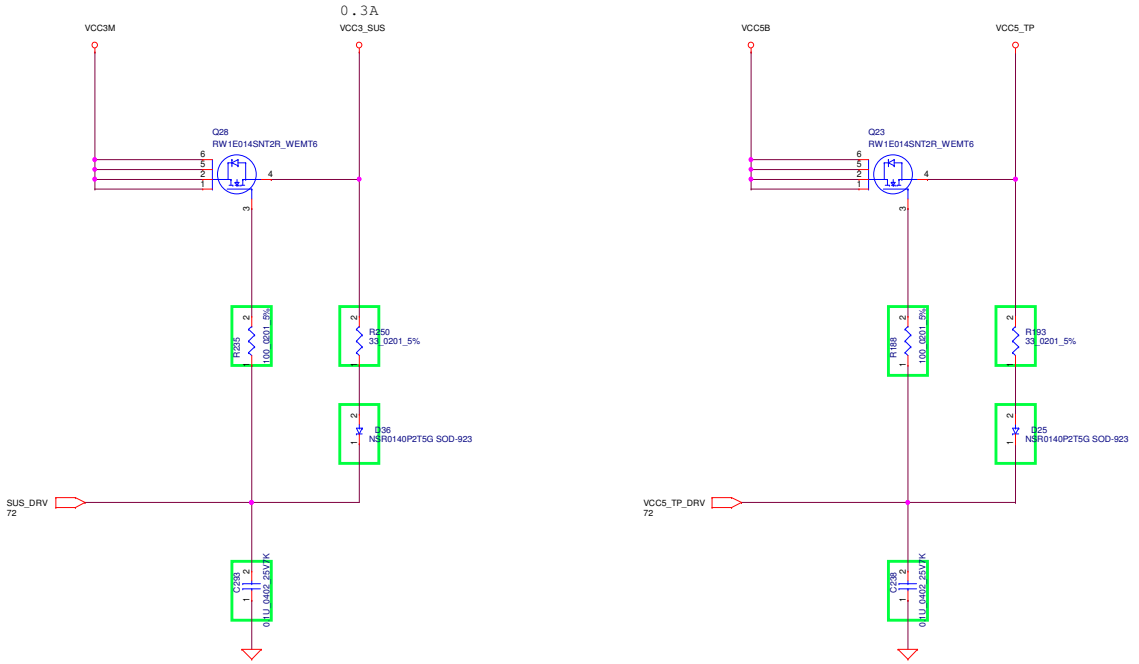

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Title: **LOAD SW PCH SUS**

Size	Document Number	Rev
Custom	Cobain SWG	0.24

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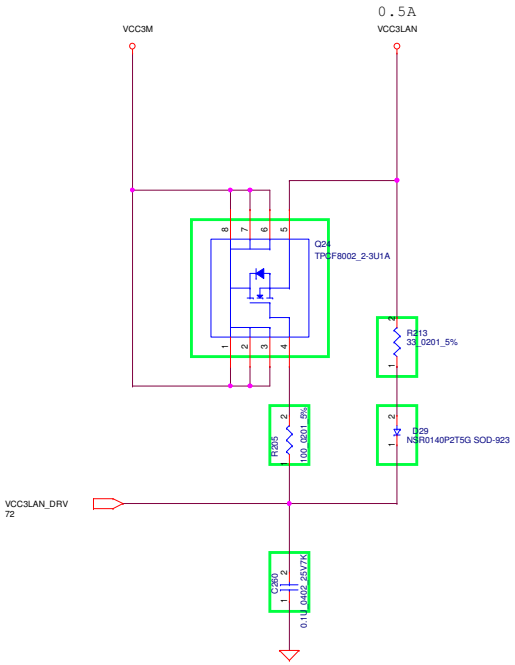

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Title: **LOAD SW LAN**

Size	Document Number	Rev
Custom	Cobain 3	0.24

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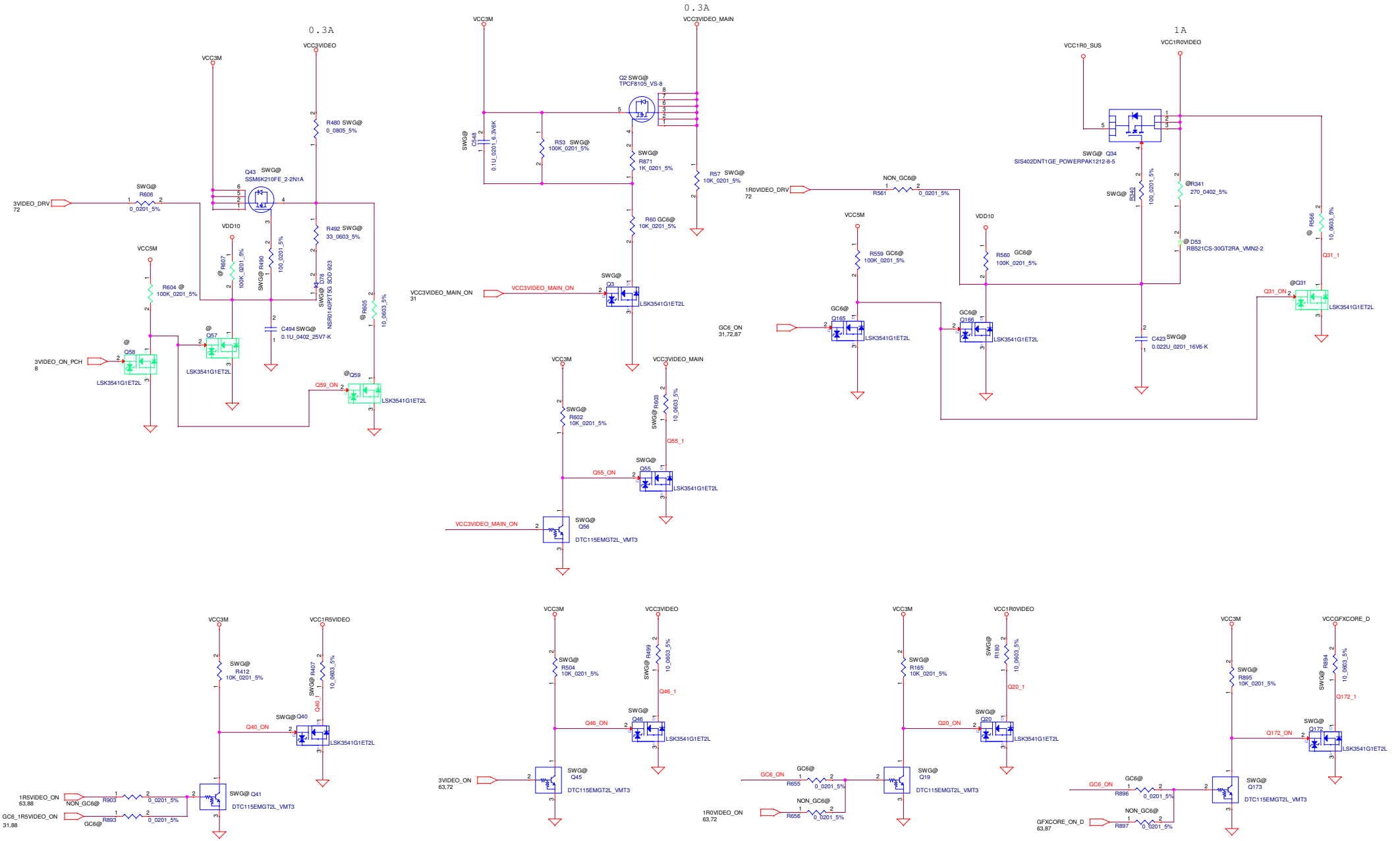

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Title: **LOAD SW VIDEO**

Size	Document Number	Rev
Custom	COBAIN3	0.24
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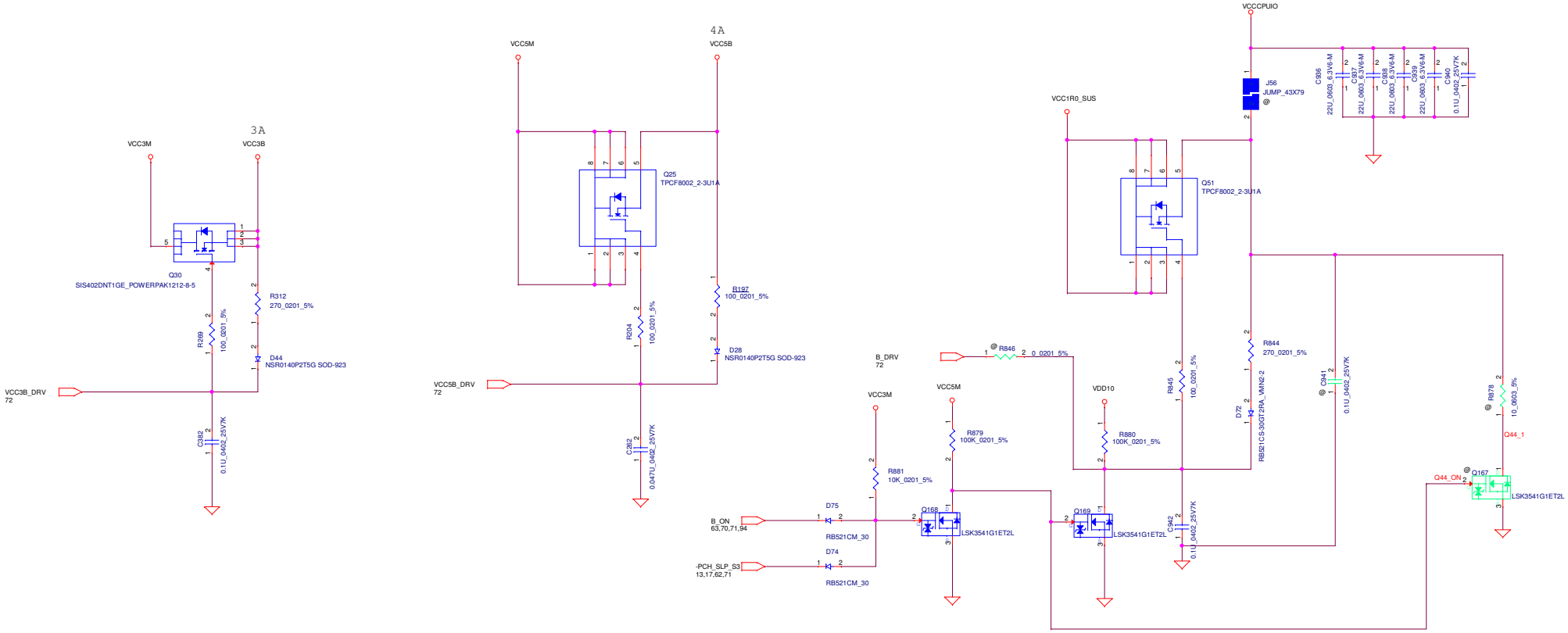

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Title: **LOAD SW B**

Size	Document Number	Rev
Custom	Cobain3	0.24

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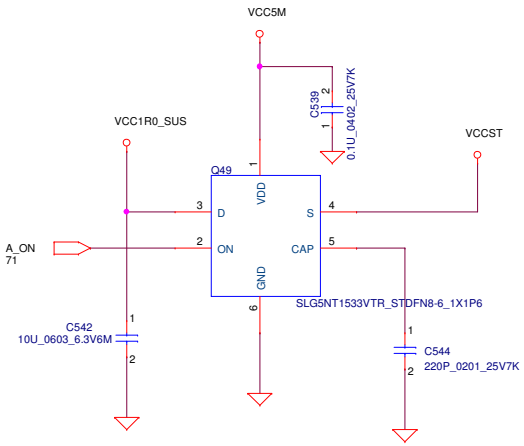

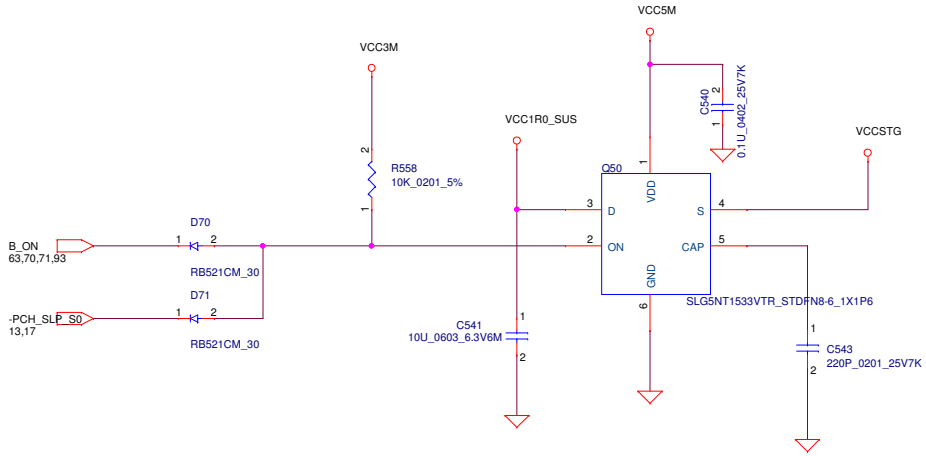

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Title: **LOAD SW CPU**

Size	Document Number	Rev
Custom	Cobain 3	0.24

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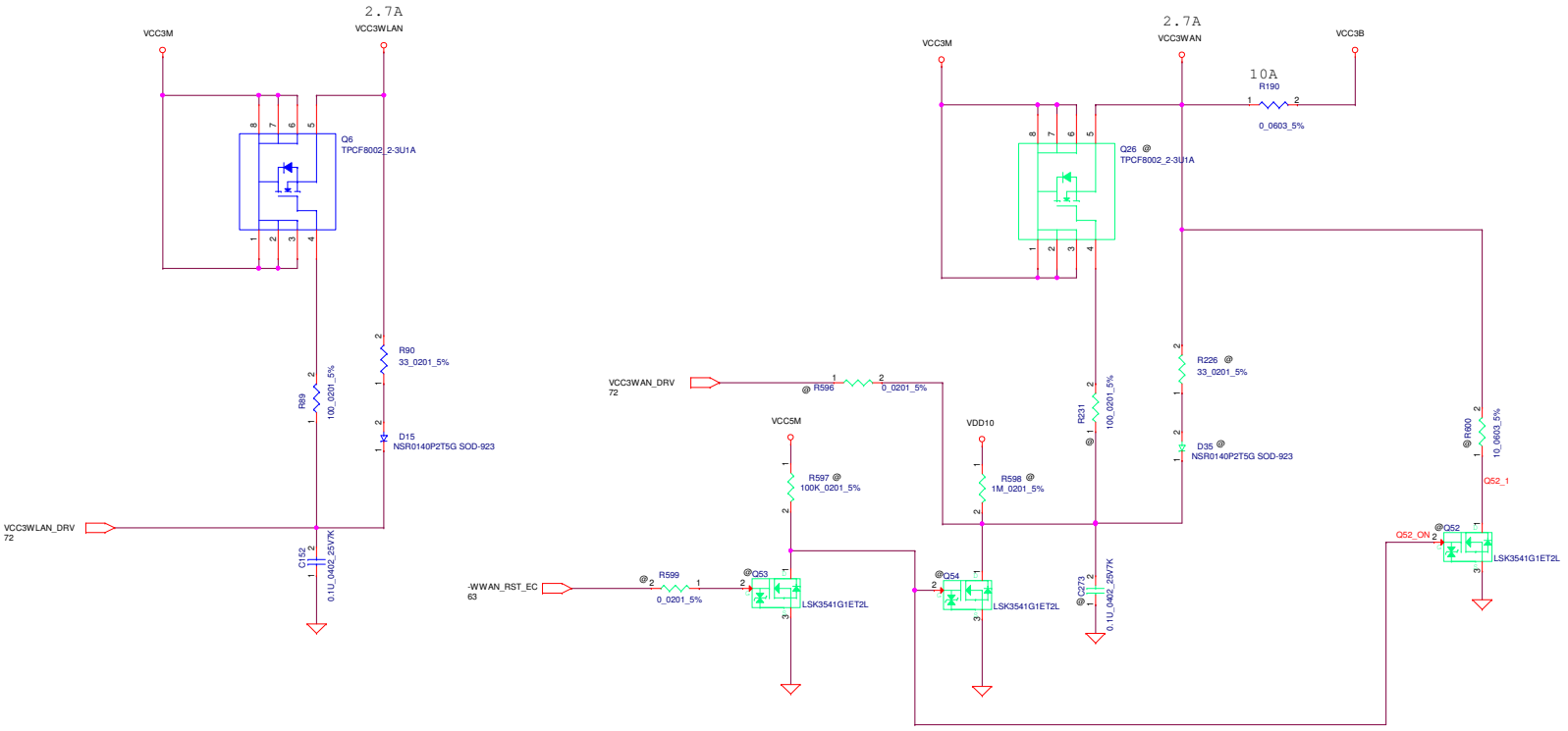

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Title: LOAD SW WWAN & WLAN

Size	Document Number	Rev
Custom	Cobain SWG	0.24
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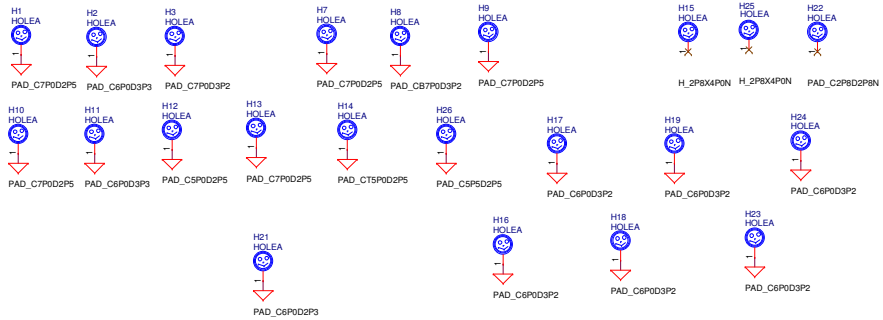
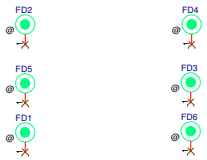


FID
Board Area



FID
Component Area

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Title: PTH FOR SCREW HOLES

Size	Document Number	Rev
Custom	COBAIN SWG	0.1

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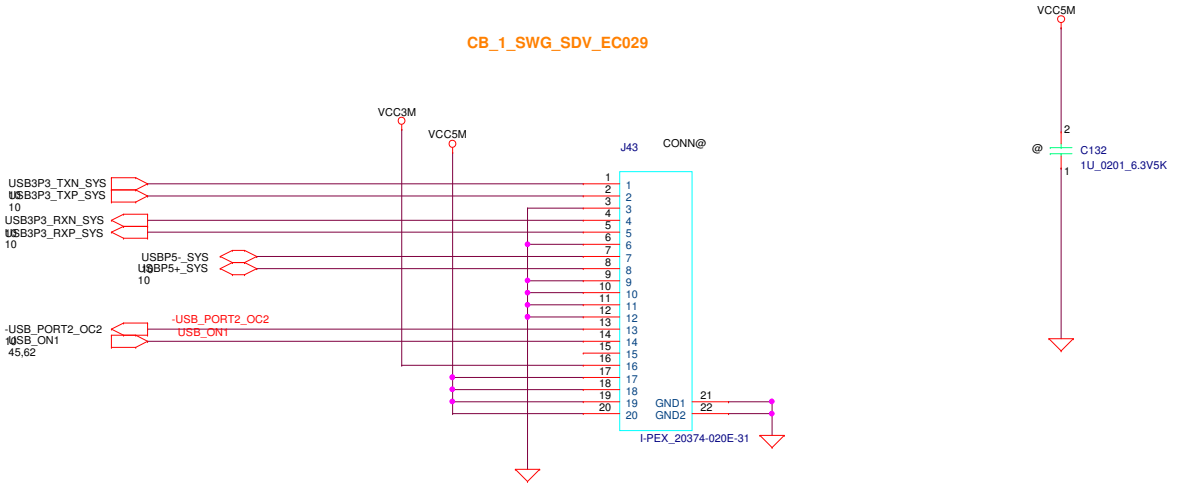

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Size: Custom	Document Number: COBAIN3		Rev: 0.24
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